3D CMOL Memristor Circuit for Analog/Neuromorphic Computing

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Memristor has surfaced as a promising component for novel analog/neuromorphic computing hardware. Stacking multiple memristor crossbar layers is an effective approach to increase the packing density, but the fabrication is challenging and the device access is limited. Here we designed and experimentally demonstrated a novel 3D memristor circuit implementing CMOL (CMOS + molecular) like architecture. The layout of the 3D circuit is optimized for the fabrication process in which only two sets of photomasks are needed for stacking multiple device layers. 3D circuits with 8 layers of memristor crossbars are demonstrated, which, to the best of our knowledge, sets a world record in 3D memristor circuit. Meanwhile, simulation shows that our design can achieve better tolerance to sneak path problem than the conventional stacked crossbar arrays. The area-distributed interconnects also enable operation of multiple sub-arrays in the 3D circuits simultaneously and independently, opening avenue for 3D convolutional neural network with flexible design.

The proposed 3D memristor system adopts a CMOL-like architecture[2] (fig. 1). The memristor array and CMOS peripheral circuits are connected through area-distributed interfaces. This novel architecture provides several unique advantages over the conventional 3D circuits. First, two pairs of independent row/column decoders are used for bottom (blue) and top (red) electrodes which map each memristor into a huge four-dimensional address space. The fourth power of the address provides the 3D system with almost infinite stackability (fig.1). Meanwhile, such unique layout makes it possible to divide large array into small segments and thus reduces the wire resistance to achieve faster speed and lower power consumption. Furthermore, by dividing the large array into small segments, the sneak path problem is not as severe because the array size is smaller. This relaxes the requirement in device properties such as high non-linearity. For example, in a 4Mb (2000 x 2000) array (typical block size of the NAND Flash), device current-voltage nonlinearity > 10^6 is required in a conventional crossbar array to achieve a reasonable output sensing margin (fig.2). By using our design with segmented sub-array, the device nonlinearity can be four orders of magnitude smaller.

3D memristor circuit with 8 monolithically integrated memristor layers is demonstrated using E-beam lithography. A nonlinear TiO_2/Al_2O_3 based memristor is developed for the 3D circuit and shows good current-voltage nonlinearity >50 (fig.3a), which is sufficient for a sub-array of 8 x 8 crossbar (fig.3b). The SEM images of the fabricated 3D CMOL circuit is shown in Fig.4. Electrodes in different device layers were connected through area-distributed vias (fig. 4c). The bottom electrodes of memristors were rerouted to new locations in the upper layers where the top electrodes were stacked vertically (fig. 4a,d). In this way, unique access to each memristor device in the 3D circuit is achieved. To provide a flat surface for each device layer, flowable oxide (FOX-15 from Dow Corning) was used to achieve layer-layer passivation and planarization. Because of the highly-correlated structure in each device layer, the same layout can be repeatedly used for every two layers and thus greatly reduce the design complexity and fabrication cost.

[1] J. J. Yang *et al*, *Nat. Nanotechnol*. **8** 13–24 (2013)
2. D.B. Strukov and R.S. Williams, *PNAS*, **106** (48), 20155-20158 (2009)

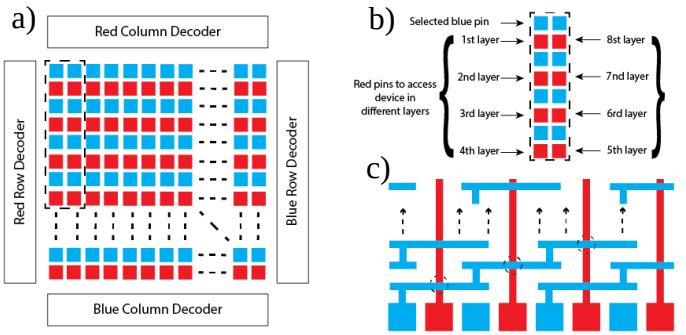

Figure 1: (a) Schematic of area distributed interface and the layout of CMOS peripheral circuit (b) accessing diagram for memristor in each layer. (c) Schematic of the stacking flow inside our 3D CMOL structure.

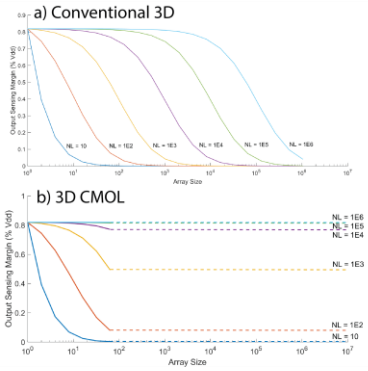

Figure 2: Simulation of worst-case output sensing margin of memristor with different nonlinearity inside large crossbar array. a) Conventional 3D Crossbar array (b) 3D CMOL with 8 layer devices

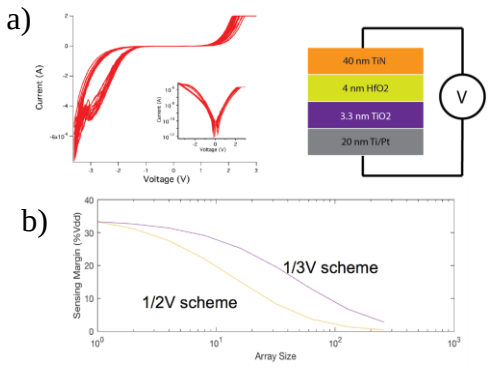

Figure 3: (a) developed high nonlinear memristor device for 3D circuit. (b) Simulation of its performance inside large array with 1/2V and 1/3V sensing scheme.

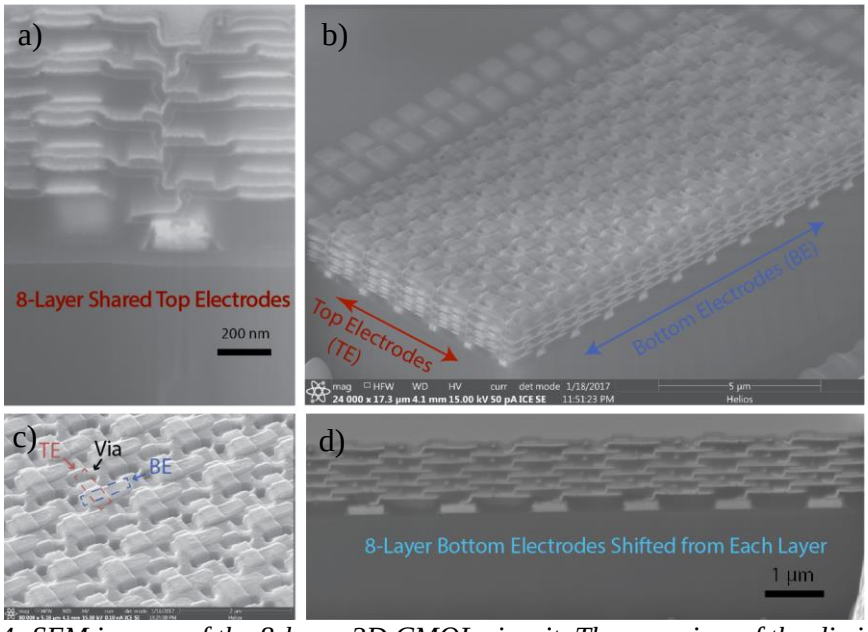

Figure 4: SEM images of the 8-layer 3D CMOL circuit. The overview of the die is shown in (b) with magnified cross-sectional images of top electrodes shown in (a) and bottom electrodes shown in (d). The tilted SEM image of the 3D circuit is shown in (c).