Fabrication of 2 x 2 nm^2 Cross-Point Memristor Array of 3.82 $Tbit/inch^2$ Packing Density

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Memristor is a two terminal device with its resistance state depending on the applied electric voltage and/or current history. Its unique electrical properties make it attractive for applications in emerging storage/memory, non-conventional computing, wireless communications etc[1-3]. However, the future success of memristor as a beyond CMOS solution relies heavily on its scalability[4]. Here, we present a novel technique to build ultra-small memristors with ultra-high packing density in crossbar arrays. We developed new methods for 2 nm feature patterning and interconnections, and addressed challenges in programming/reading of the arrays.

To reduce series resistance of the nanowire electrodes, we increased the wire aspect ratio to over 1000 by depositing metal thin films on a sidewall. We built 2 nm Pt electrodes of 4.5 um height (Fig. 1) that provided orders of magnitude lower wire resistance (<65 Ω/μm) as compared to that of a previously reported Cu wire (>10^7 Ω/μm for a 5 nm Cu wire[5]). This low series resistance may enable >1Mb array even with such small feature size[5].

We fabricated arrays of 2 nm wide metal nanowires (13 nm pitch) by alternatively depositing Pt and ALD of Al_2O_3 isolation layers in between. SEM image in Fig.2 shows the top view of one such electrode array. Two 2 nm wide electrodes were built with 13 nm pitch in close neighbor to an 8 nm wide electrode for comparison. These 2 nm electrodes were confirmed to be electrical conductive but also isolated from each other.

Finally, we built a 3 × 3 cross-point memristor array by stacking two of such 2 nm electrode arrays orthogonally with an oxide switching medium inserted in between (Fig. 3). With the 13 nm pitch, the packing density of the array is 3.82 $Tbit/inch^2$. This result not only sets a solid platform to examine memristive switching behavior at atomic-scale/high-density, it provides great opportunities to study the ultimate scaling limitation for emerging info processing technologies.

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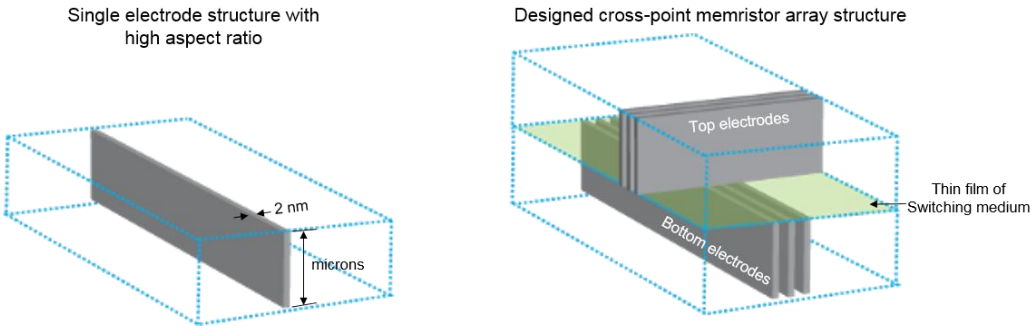

Figure 1: Schematics of device structures: a single electrode with high aspect ratio (drawn not to scale) is displayed on the left. Right figure shows a 3 × 3 cross-point memristor array structure built on top of such electrode. The dotted wire frames indicate the supporting substrates.

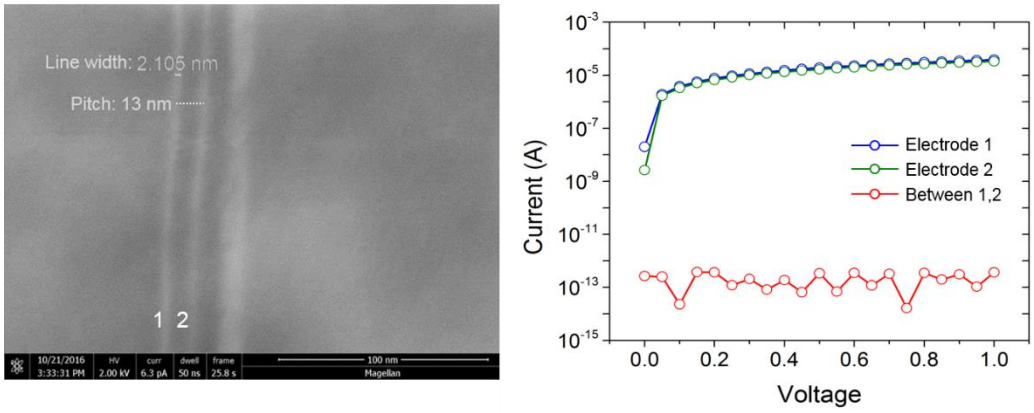

Figure 2: 2 nm electrode array: SEM image on the left shows a top view of the 2 nm electrode array made in 13 nm pitch (the third electrode was made wider to demonstrate the ability of line width control). I-V curves measured from electrode #1 and #2 in the SEM image were plotted on the right. The red curve indicates the good insulating between electrode 1 and 2.

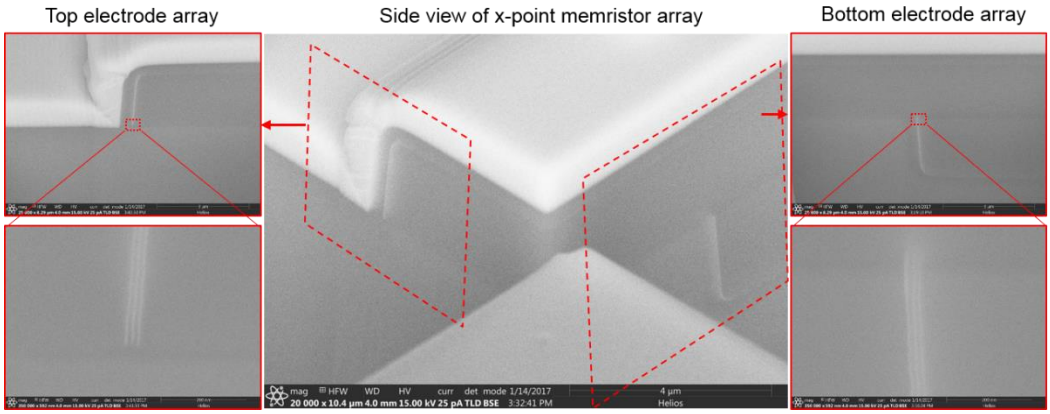

Figure 3: High density 2 nm cross-point memristor array: SEM in the middle panel shows the overall structure of a 3 × 3 cross-point memristor array. Left and right panels display zoom-in images of the top and bottom electrode respectively. This cross-section sample was prepared by FIB. The SEM images were captured by the same dual beam machine with limited resolution for fully resolving the 2 nm electrodes' line width although the 13 nm pitch was still measurable.