

Low-thermal-budget surface preparation for STM Lithography

J. H. G. Owen, J. Ballard, R. Santini, J. N. Randall and J. R. Von Ehr
Zyvex Labs LLC, 1301 N. Plano Rd, Richardson, TX 75081, USA.

S.Sando and S. J. Anz,
Systine Inc., Pasadena, CA

jowen@zyvexlabs.com

Applications of STM lithography such as nanoimprint masters grown by ALD, or buried nanoelectronic devices, place stringent requirements on the Si(001):H surface preparation. The standard preparation methods, involving flash heating to 1200°C, causes surface roughness on the μm -scale which is too great for the nanoimprint process, and which will damage any alignment marks or mesoscale electrodes placed on the surface.

We have developed a lower-temperature process which still provides atomically flat, clean surfaces, but with a maximum sample temperature of 700°C. The process involves two steps: a H cleaning process to remove surface hydrocarbons before removal of the oxide film [1] and then surface oxide removal using a flux of silicon onto the outside of the oxide film. The Si reacts with SiO_2 , to form SiO, which is volatile at this temperature [2].

For the H clean, we use an atomic hydrogen source from MBE Komponenten to provide a large flux. At a background pressure of 7×10^{-6} Torr, a cleaning time of 40-60 minutes is sufficient to prevent the formation of SiC particles on the surface. As shown in Fig. 1, the H clean also appears to affect the oxide thickness. The front of a sample exposed to the H flux lost all of its oxide, whereas the back did not. The annealing time can be reduced by bombarding with a combination of electrons from an electron source along with the atomic H or by replacing the two separate fluxes with a H DC plasma, as in the Low Energy Electron Enhanced Etching (LE4) process. During the oxide removal step, there is a competition between Si supplied from the flux and Si supplied from the Si/oxide interface. If substrate Si is consumed, deep pits form at the interface, resulting in a very rough surface. We have found that a Si flux of about 1ML/s allows a flat surface to be formed. Examples are shown in Fig.2.

However, at the source temperature required to achieve this flux, some metal contamination of the evaporated Si occurs. The resulting defects cause background nucleation for hard mask growth using ALD. To prevent this, we are investigating the use of disilane as a gas-source precursor for the required Si.

[1] A. Aßmuth, T. Stimpel-Lindner, O. Senftleben, A. Bayerstadler, T. Sulima, H. Baumgärtner, and I. Eisele, *Appl. Surf. Sci.*, vol. 253, pp. 8389–8393, 2007.

[2] G. D. Wilk, Y. Wei, H. Edwards, and R. M. Wallace, *Appl. Phys. Lett.*, vol. 70, no. 17, pp. 2288–2290, Apr. 1997.

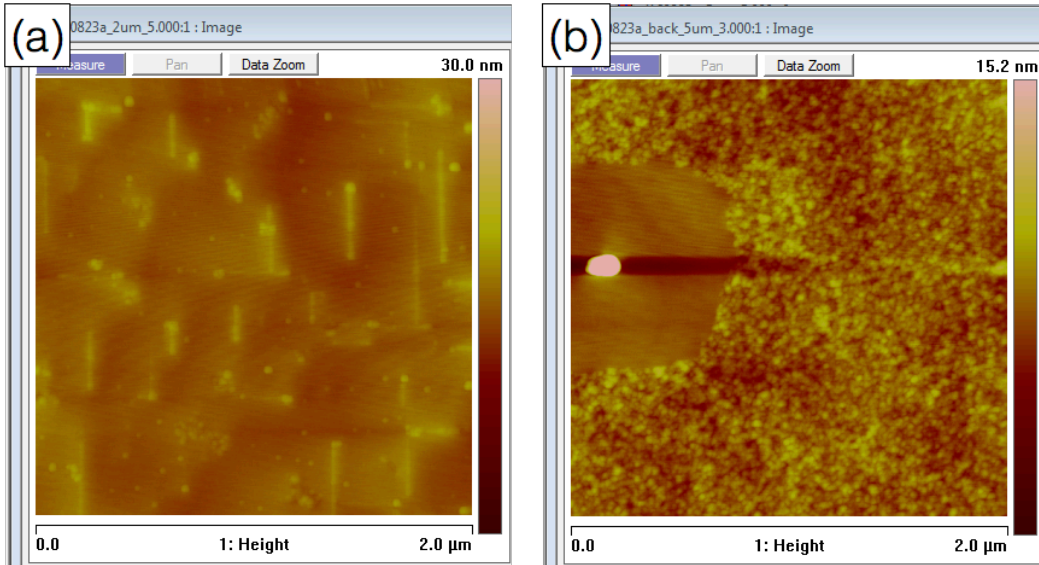


Figure 1: Effect of H flux on oxide. (a): Front, exposed to atomic H flux for 20 mins, showing SiC features. (b): Back, same sample, not exposed to atomic H flux, showing partial oxide removal in crater. The sample was annealed after the H clean for 20 mins at 800°C, then 20 mins at 900°C to thermally remove oxide. The front, exposed to the atomic H flux, has lost all of its oxide, whereas the back still has remaining oxide.

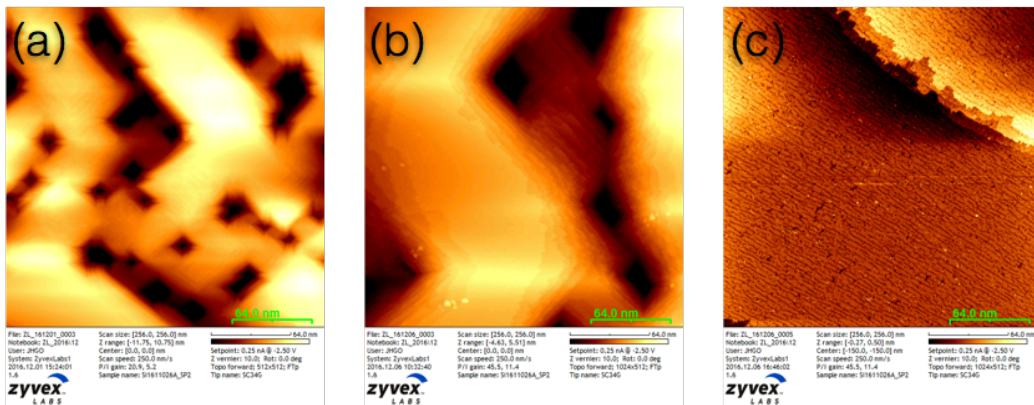


Figure 2: Effect of Si flux on surface morphology after oxide removal. Evaporation source temperature: (a) 1100°C (b) 1150°C (c) 1200°C. For lower fluxes, Si is consumed at the Si/oxide interface, causing deep pits to form. For high fluxes, a flat surface is created, without pitting.