

Process Simulation of Si Dot Fabrication for SETs by Ion Beam Mixing and Phase Separation in Nanopillars

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The single electron transistor (SET) is considered a promising candidate to continue the revolution of information technology due to its very low energy consumption (~100 times less than common FET). The big challenge is the manufacturability of SETs working at room temperature (RT). This requires the fabrication of much smaller structures (<5nm) than present-day and even future (multi-E-beam or EUV) lithography can provide.

Here we propose an ion-beam-assisted, CMOS compatible fabrication process of SETs. To realize the controlled tunneling of single electrons we propose a nanopillar of a Si/SiO₂/Si stack with a single Si quantum dot embedded in SiO₂ and connected by tunnel junctions to Si electrodes, which makes the drain and source. For RT operation the quantum dot has to be smaller than 5nm and requires tunnel distances lower than 2nm. The size of this pillar needs to be in the range of 10-20nm.

In this presentation we show the simulation of a CMOS compatible process to fabricate this quantum dot by using ion beam mixing and self-assembly. Earlier projects¹ proved already the reliability of dot formations using ion beam mixing technologies. Starting with a layerstack of Si/SiO₂/Si, the ion beam irradiation by high energy Si⁺ ions causes mixing of the two Si/SiO₂ interfaces what transforms the SiO₂ layer into metastable SiO_x (Figure 1). During subsequent heat treatment the mixed region of SiO_x (<10nm²) separates into Si and SiO₂, what leads to the formation of one single Si nanodot in the SiO₂ layer (Figure 2). The irradiation simulations are done by TRIDYN² and TRI3DYN³ program codes and the annealing by a self-developed Kinetic Monte Carlo program. We will present, how this process can be controlled using the ion beam irradiation values, geometrical sizes and the heat treatment parameters, so that it is yielding suitable conditions for application in hybrid SET-CMOS devices operating at RT.

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¹ L. Röntzsch, et al., phys. Stat. sol. (a) 202, 15, R170-R172 (2005)

² W. Möller, W. Eckstein, Nucl. Instr. and Meth. in Phys. Res. B2 (1984) 814

³ W. Möller, Nucl. Instr. and Meth. in Phys. Res. B, vol. 322, 23-33 (2014)

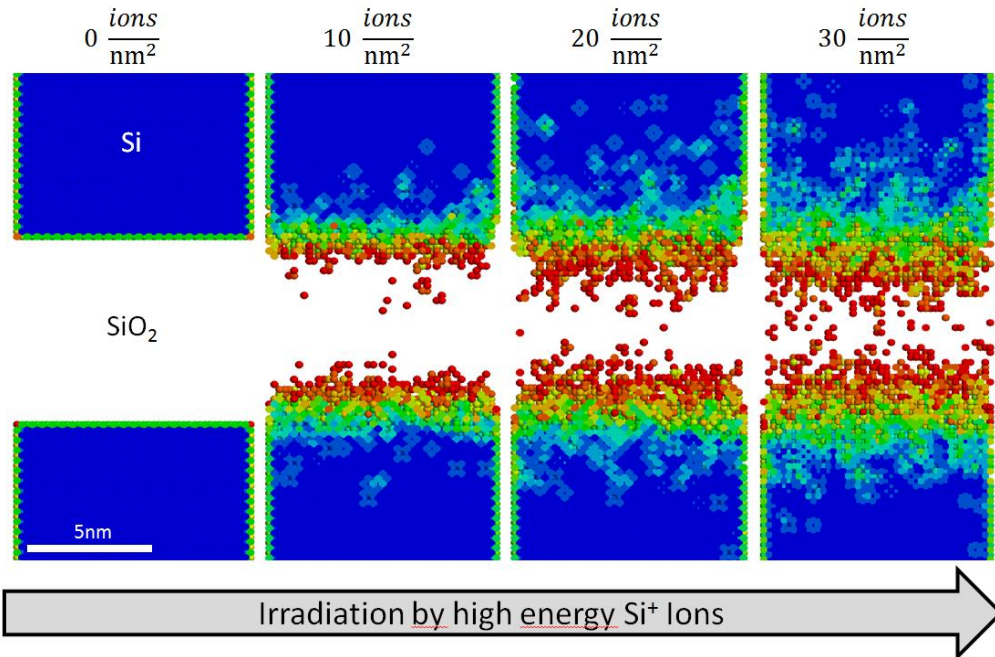


Figure 1: A cut through a Si nanopillar with a 7nm thin SiO₂ layer: The simulated mixing at the Si/SiO₂ interfaces with increasing 50keV Si⁺ fluences is shown.

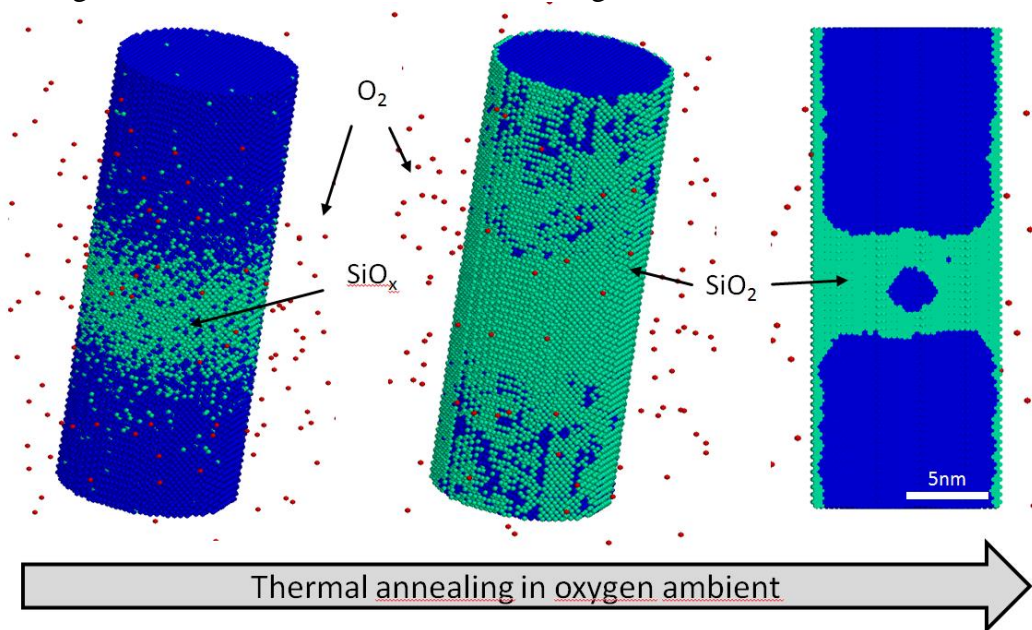


Figure 2: Simulation of the thermally activated phase separation in the ion beam mixed nanopillar: At appropriate Si⁺ fluences, pillar sizes and SiO₂ layer thicknesses, a single Si quantum dot self-assembles. Self-assembly is supported by simultaneous oxidation forming the oxide for the gate-all-around nanopillar SET.