Spatially controlled fabrication of individual silicon nano clusters using ion beam mixing and thermal treatment

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The miniaturization of computing devices and the introduction of the internet of things creates an increasing demand for the development of low power devices. Single electron transistors (SETs) are very low power dissipation devices and thus ideally suited for this demand. Combined with existing CMOS technology which is characterized by high speed and driving the existing draw backs of SETs are compensated. The development of such hybrid SET-CMOS devices is currently hindered by missing large scale manufacturing routes. For room temperature (RT) operation it is necessary to create a single nanocluster with a diameter below 5 nm exactly positioned between source and drain at a tunnel distance of only a few nanometers.

We show the first results on the way to a CMOS compatible fabrication process based on ion beam mixing and self-assembly to form a Si cluster with a size below 5 nm. Our process ensures that (a) the cluster size is small enough to allow RT operation, (b) the cluster is located at the correct tunnel distance between source and drain, (c) the clusters form at predetermined locations, and (d) the process is CMOS compatible. These goals are reached by a combination of localized ion beam mixing and a carefully tuned thermal treatment that leads to a self-assembly process that guarantees (a) and (b). In this initial demonstration of the single cluster formation process we utilize a Helium Ion Microscope to locally mix Si into a buried oxide layer. The highly focused Ne beam available in this instrument allows point like irradiation and hence reduces the mixing volume to $(10nm)^3$. Subsequent annealing results in the formation of a single 2 nm Si cluster located less than 3 nm from the adjacent Si/SiO_2 interfaces. Energy-filtered TEM (EFTEM) (Figure 1) has been utilized to reveal the presence of individual clusters. For a CMOS compatible fabrication process the restriction of the collision cascade and therefore the ion beam mixed volume will be realized by using broad beam irradiation of nanopillars with an embedded oxide layer and a diameter below 20 nm. The aim is to fabricate gate-all-around nanopillar RT-SETs together with state-of-the-art FETs. TRI3DYN and kMC simulations (Figure 2) are used to study these future works and compare them to the above discussed study based on focused ion beam irradiation.

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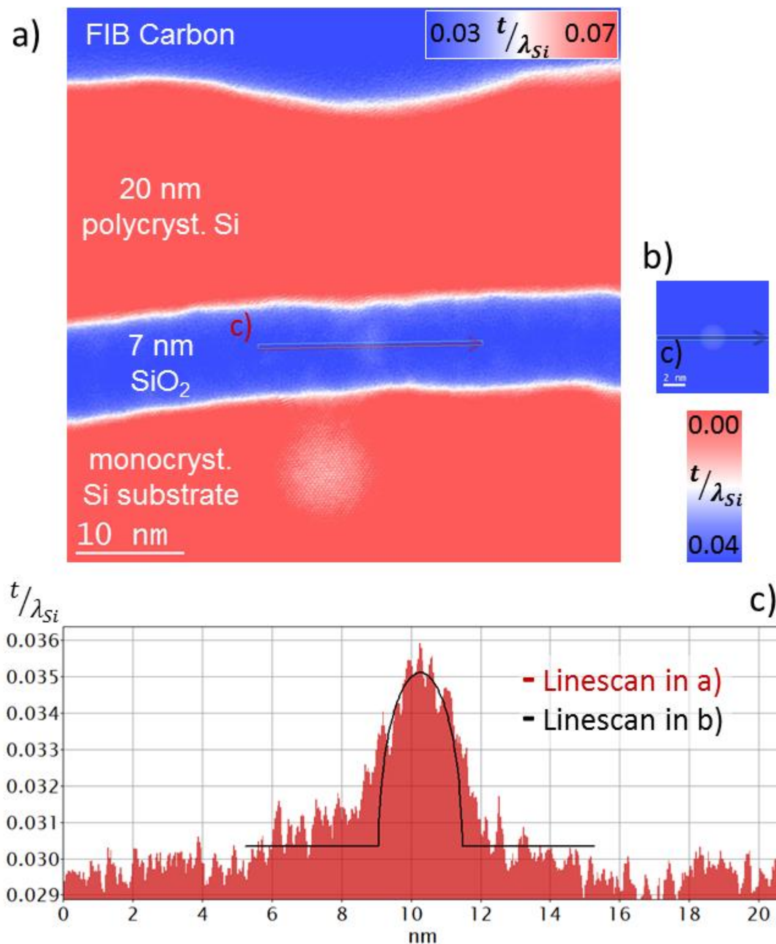

Figure 1: EFTEM analysis of single Si cluster: (a) thickness t over mean free path length λ_{Si} gained from an EFTEM image of a single Si cluster in SiO_2. (b) Simulation of the expected contrast of a single 2 nm Si cluster. (c) Intensity profile along the indicated line in (a) showing the size of the cluster and comparison to the expected intensity profile obtained from (b).

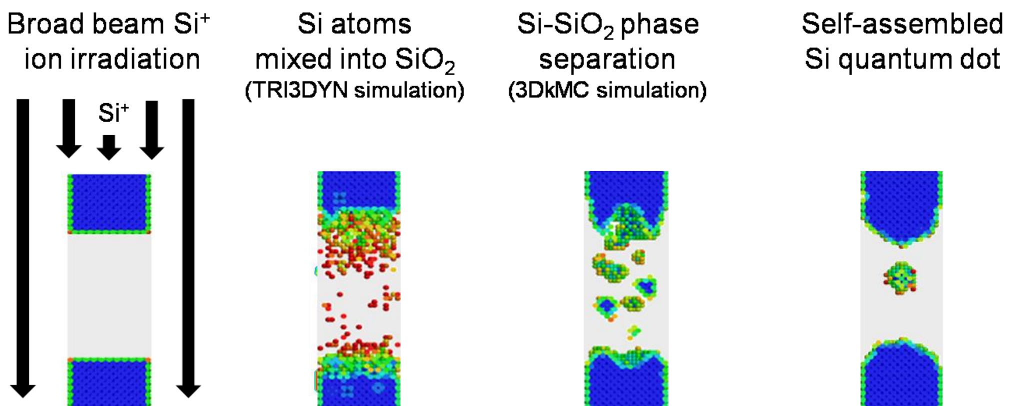

Figure 2: Simulation results: TRI3DYN and kMC Simulation results showing the formation of a single Si cluster in a Si pillar with an embedded SiO_2 layer.