Graphene Oxide Thickness Effects in Graphene-based Supercapacitors

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Due to its unique characteristics – high electrical conductivity and large surface-to-volume ratio – graphene has been explored as an electrode material in the development of supercapacitors. These graphene-based supercapacitors exhibit very high capacitance values compared to those of conventional capacitors. In this study, the thickness effects of the graphene oxide (GO) layer used in the graphene-based supercapacitors was examined.

Three sets (A, B, and C) of graphene-based in-plane interdigital supercapacitors were constructed, each with a different GO thickness. Each set consists of six capacitors. The structure of each capacitor is illustrated in Figure 1. The thickness of the GO layer for sets A, B, and C is 3.43 μm, 4.86 μm, and 8.01 μm, respectively. These GO layers were thermally reduced to graphene (rGO) using a laser engraver. The capacitors were evaluated with the Gamry 1000E Potentiostat. A typical cyclic voltammetry (CV) graph is depicted in Figure 2. ANOVA tests were performed on the resulting capacitance and specific capacitance (C/cm^3).

Capacitors with a thicker layer of GO yielded a higher average capacitance than those with a thinner GO layer. The average capacitance for the three sets is 5.65 mF, 6.44 mF, and 8.07 mF, respectively. These results were deemed statistically significant with a p-value of 0.028. Calculation of the specific capacitance showed that using a thinner layer of GO yields a higher specific capacitance. Sets A, B, and C had average specific capacitance of 10.9 F/cm^3, 8.80 F/cm^3, and 6.70 F/cm^3, respectively. With a p-value of 0.013, these results were found to be statistically significant as well.

Greater specific capacitance can be achieved from capacitors with thinner GO layers. Capacitance can be more effectively increased by the variation of the thermal reduction process. Using the same laser engraver settings to reduce different thickness GOs produced different porosity and different finger separations as shown in Figure 3. The process of thermal reduction of GO using a laser engraver is studied and the results are presented in this paper.

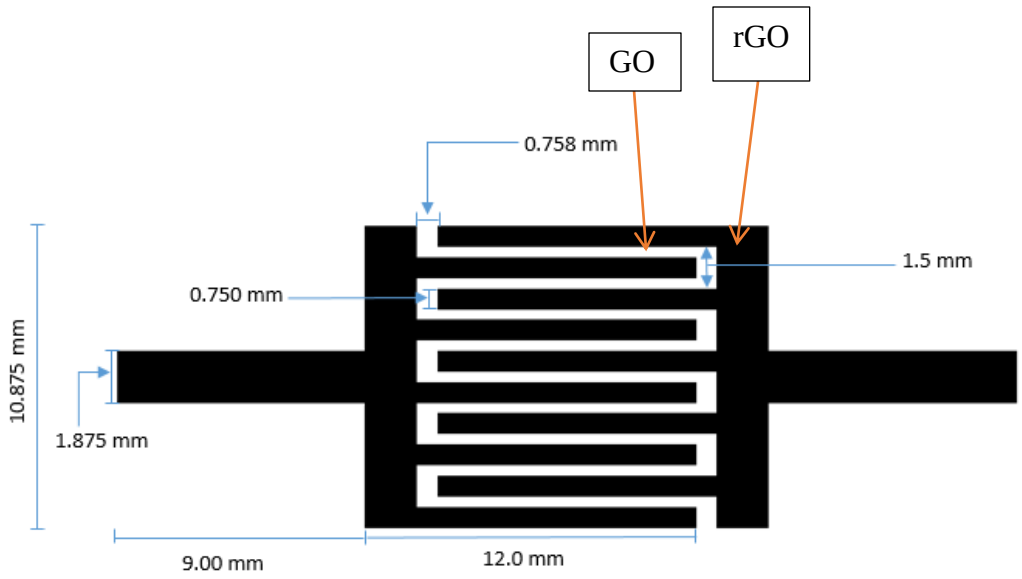


Figure 1: The in plane interdigital supercapacitor structure

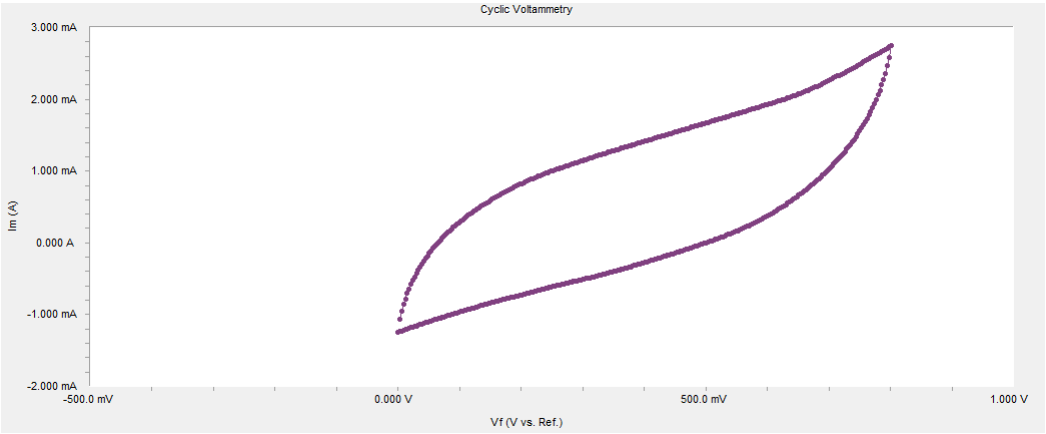
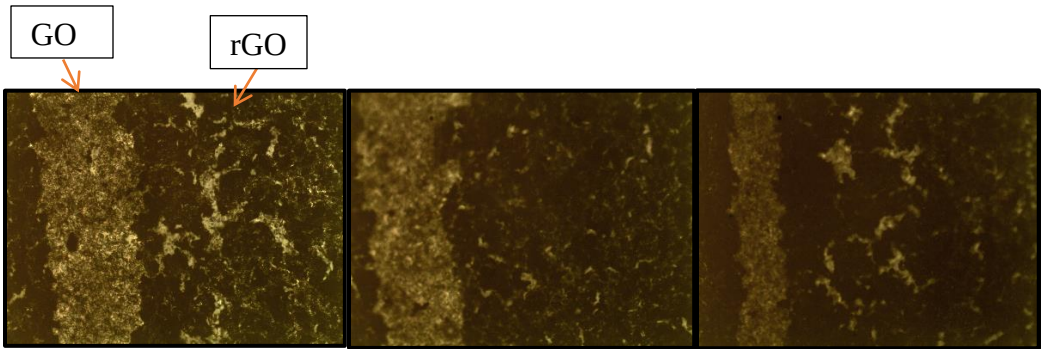


Figure 2: Cyclic voltammetry graph of a capacitor in set A



Set A Set B Set C

Figure 3: Microscope images of the capacitors