Physically Unclonable Anti-Counterfeit Labels Using Nanoscale Diffusive Memristor Crossbar Arrays

Rui Zhang[1,2], Hao Jiang[1], Peng Lin[1], Zhongrui Wang[1], J. Joshua Yang[1], Daihua Zhang[2], Qiangfei Xia[1*]

1. Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, MA 01003;
2. College of Precision Instrument and Optoelectronics Engineering, Tianjin University, Tianjin 300072

E-mail: qxia@umass.edu

Information security is a critical issue in the era of Internet of Things (IoT) when the number of devices that are connected together is exponentially growing. Physical unclonable functions (PUF) have emerged as promising candidates for anti-counterfeit labels, for their intrinsically random feature is easily evaluated but impractically duplicated. Optical PUFs[1] are able to achieve large number of challenge response pairs (CRPs), but they require laborious setup and complicated post-processing of data. On the other hand, intrinsic electronic PUFs do not involve post-processing and are fully compatible with CMOS technique, but most of them suffer from side-channel attack, limited security density and complicated fabrication process[2].

Here, we present a novel PUF using nanoscale diffusive memristor[3] crossbar arrays that can be fabricated with much simpler process and higher fabrication controllability. Our PUF utilizes the random distribution of Ag particles on a SiO_2 surface generated during sputtering process, showing high security density and reduced power consumption.

As illustrated in Figure1 (a), a diffusive memristor array consists of two sets of Au electrodes sandwiching a switching layer of SiO_2 embedded with Ag nanoclusters. 15 nm Au/Ti bottom electrodes (BEs) and 40 nm Au top electrodes (TEs) were patterned via e-beam lithography, followed by evaporation and lift off process. The 20 nm Ag/SiO_2 film was deposited via co-sputtering. The diffusive memristors exhibit volatile switching behavior. A sweep voltage of 1.8 V with a compliance current of 100 nA sets the device from high resistance ("0") to low resistance state ("1") (Fig. 1b). After removing the voltage, the memristor relaxes back to its high resistance state automatically, and hence is more energy efficient.

Figures 2(a)-(c) show fabricated memristor crossbar arrays with various electrode width (100-300 nm). We use "switch-on" device yield and inter-Hamming distance to evaluate the performance of our PUF, the ideal value of which are both 50%. By varying electrode width or Ag sputtering power, various "turn-on" device yields were achieved. As illustrated in Figure2 (d) and (h), devices with 100 nm electrode width and a switching layer sputtered with 10 W DC power on Ag target have the optimized device performance. The switch-on yield and the inter-Hamming distance is 51.2% and 49.72%, respectively. A 16×20 random binary bits map was then constructed (Fig. 3a) for 320 devices in the 100 nm memristor array. The distribution of the inter-Hamming distance is found to be centered at 0.5068 with a variance of 0.0110 (Fig. 3b). The intra-Hamming distance (among different arrays) and device retention time at higher temperature (e.g., 85 ºC) will be evaluated.

[1] Smith A F *et al*. *Adv. Funct. Mater.* **26**, 1315-1321 (2016).

[2] Herder, Charles, *et al. Proc. IEEE* **102** 1126-1141 (2014).

[3] Wang, Zhongrui, et al. *Nature materials* **16** 101-108 (2017).

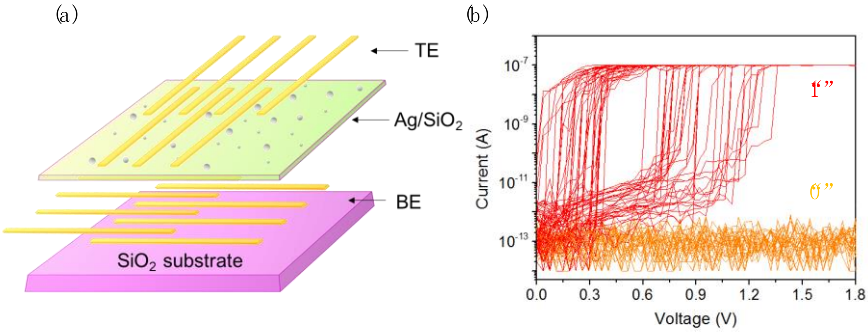

Figure1. (a) Schematic of device fabrication. (b) I-V curves of diffusive memristor arrays. The 'switched-on' devices are represented by 1 while the others are represented by 0.

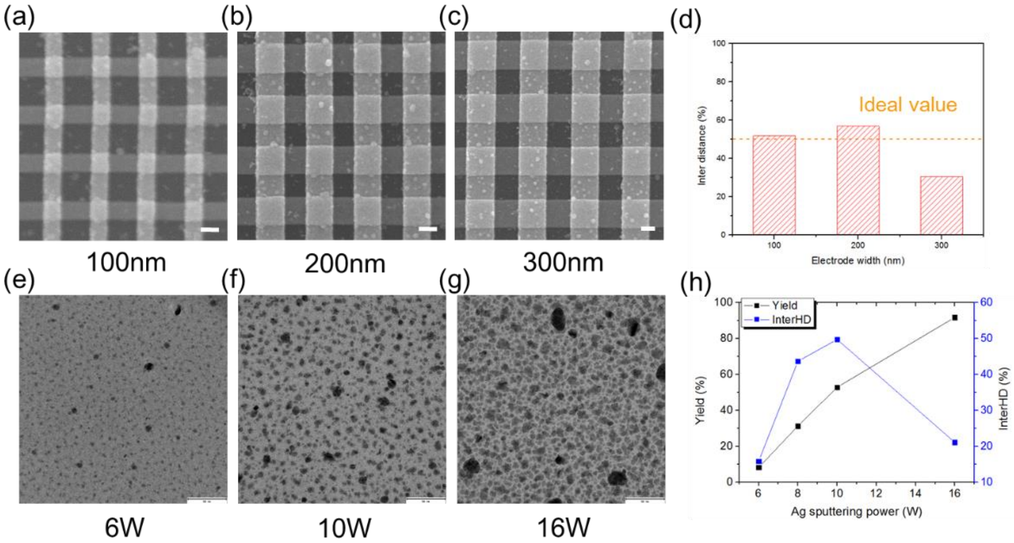

Figure2. (a)-(c) SEM images of diffusive memristors arrays with different electrode widths. The scale bars are 100nm, 100nm and 150nm, respectively. (d) Electrode-width dependent inter-distance calculated from I-V measurement results. (e)- (g) TEM images of diffusive memristors with different Ag sputtering power. (h) Ag sputtering power dependent yield and inter-distance extracted from I-V curves.

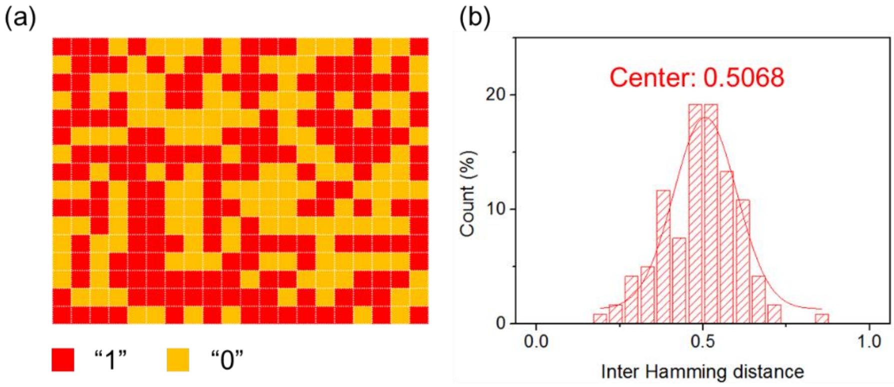

Figure3. (a) 16×20 random binary bits generated from I-V curves of memristor arrays with 100nm electrode width and 10W Ag sputtering power. (b) The distribution of the inter-distance of 16 bits binary fingerprint. The distribution is approximated with Gaussian curves and the means and variance are 0.5068 and 0.0110 respectively.