Quantifying Dopant Movement in Si:P Atomic Device Encapsulation

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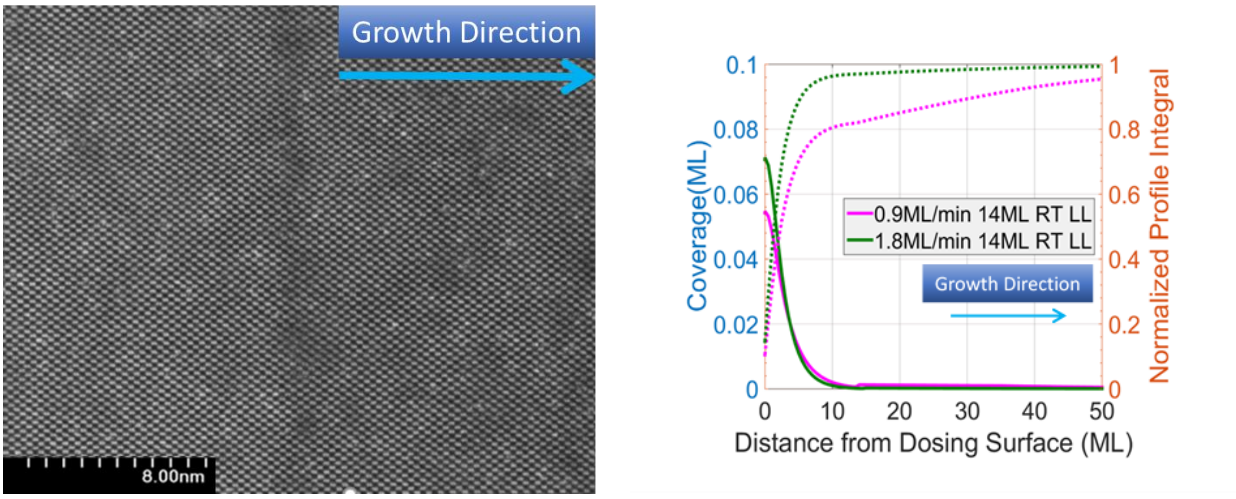
Doped semiconductor structures with ultra-sharp dopant confinement, minimal lattice defect density, and high carrier concentration are highly desirable in the development of both ultra-scaled conventional semiconductor devices and emerging all-silicon quantum computers. In addition, as semiconductor devices scale down to a sub-5 nm regime, determining exact dopant locations with sub-nm accuracy/precision becomes increasingly critical to successful device fabrication and performance. In a few-atom quantum device, atomic position accuracy is even more critical: movement of even a single lattice site can affect quantum state coupling or device energetics.

Advanced Hydrogen Lithography techniques using scanning probes have enabled deterministic placement of single phosphorus dopants into specific Si (100) surface sites followed by encapsulation in epitaxial silicon. And although atomically precise device fabrication enables atomically abrupt dopant confinement in both lateral and vertical directions, dopant segregation and diffusion during the device encapsulation process introduce large uncertainties to the exact locations of dopant atoms.

In this study, we systematically investigate locking layer effects to suppress dopant movement during low-temperature encapsulation overgrowth and to optimize dopant confinement, epitaxial quality, and transport properties of the phosphorus-doped 2D layer. We use secondary ion mass spectroscopy (SIMS), scanning tunneling microscopy (STM), transmission electron spectroscopy (TEM), and low-temperature transport measurements to elucidate the respective roles of locking layer thickness, growth rate, and thermal anneal in optimizing the delta layer quality. We quantify the delta layer dopant confinement channel thickness by extracting the actual dopant concentration profiles from SIMS results using sputter profiling modeling. We examine the effect of delta layer quality on low temperature transport measurement and use weak localization (WL) to characterization the electrical conduction channel thickness.



(a) (b)

Figure 1. (a) High-resolution cross-section TEM image at a Si:P delta layer interface fabricated with a locking layer (LL). (b) The simulated dopant concentration depth profiles (solid lines, left axis in the unit of dopant coverage per monolayer (ML)) and the normalized profile integrals that represent the total dopant incorporation probability as a function of overgrowth thickness (dotted lines, left y-axis). (1ML = 0.1384 nm in Si (100))