# High-throughput process chain for SET devices based on FE-SPL and SmartNIL$^{TM}$ technology

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Next generation electronic devices like single electron transistors (SETs) operating at room temperature demand for high-resolution patterning techniques and simultaneously high-throughput fabrication. Thereby, field-emission scanning probe lithography (FE-SPL) is a direct writing method providing high-resolution and high-quality nanopatterns. SET devices prepared by FE-SPL and plasma etching at cryogenic temperature were shown to operate at room temperature [1]. Nevertheless, FE-SPL lacks in writing speed and large area manufacturing capability required for industrial device manufacturing. This can be overcome by combining FE-SPL with nanoimprint lithography (NIL), which enables the replication of high-resolution features on large areas and provides high throughput.

In this work we will review a high-throughput process chain for SET fabrication based on reproducing FE-SPL prepared templates by NIL and etching. For a detailed analysis of the process chain the SET layout depicted in Fig. 1 was used, which includes high-resolution patterns with a distance between the channels below 50 nm. The masters for NIL were chips with a size of 1.5 x 1.5 cm². For the definition of the layout, a mix & match approach was applied. In this context, contact pads, as well as an active area for FE-SPL patterning were fabricated by optical lithography & standard reactive ion etching (RIE), while high-resolution features were patterned by FE-SPL and cryogenic RIE.

This master was replicated to a polymer working stamp. This was then used for patterning of silicon wafers by using the Hercules NIL system (shown in Fig. 4), which is capable of processing up to 200mm sized wafers and includes the SmartNIL$^{TM}$ technology covering the full imprint process chain from substrate cleaning, coating, and baking to patterning. AFM measurements of the master and imprint are depicted in Fig. 2. Subsequently the structures have been etched into the silicon substrate (Fig. 3) using 300 mm industry-compliant plasma etch systems, proving high fidelity pattern transfer into the substrate.

[1] I. W. Rangelow, et al., J. Vac. Sci. Technol. B34 (2016).

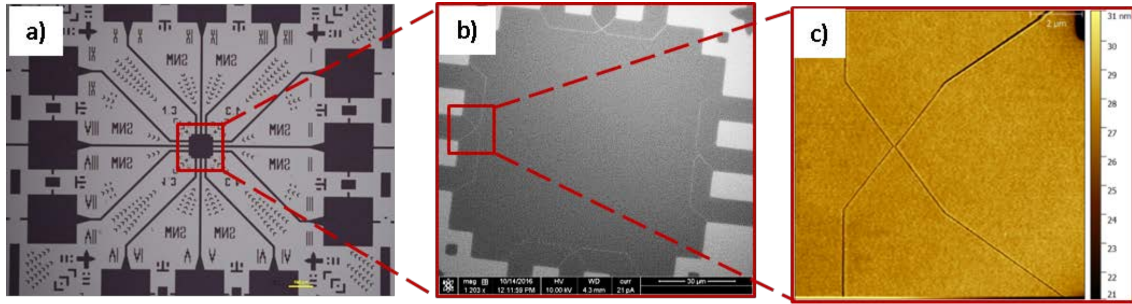


**Figure 1.** a) Optical image of one field of the SET layout including contact pads (black). b) SEM image of middle field marked in (a). c) AFM image of SET pattern marked in (b).

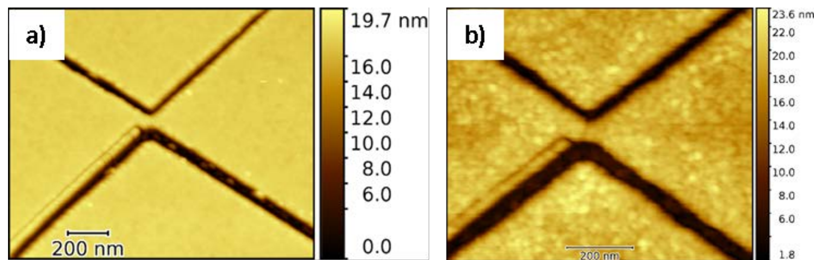


**Figure 2.** AFM image of the SET channel on the master (a) and after imprinting (b).

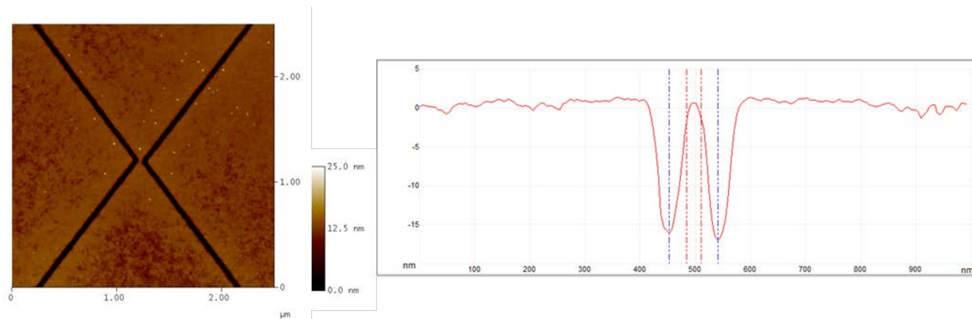

**Figure 3.** AFM image profile (through the channel) after etching using an optimized sequence for plasma descum, $SiO_2$ breakthrough and Si etch.

**Figure 4.** Hercules NIL system for fully automated nanoimprinting on 200mm Wafers including pre-processing modules.