Materials Innovation to Address the Challenges of Advanced Implant Lithography

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In recent years the complexity of device manufacture has significantly increased as a function of device node (Figure 1)[1]. This trend to increasing number of process steps (litho, etch, implant, strip etc.) is expected to continue for both logic and memory devices. From the lithography standpoint, one of the major contributors to the increasing process complexity is the large number of implant levels required for advanced devices (Figure 2)[2]. The importance of implant lithography cannot be underestimated. First and foremost, it is the process used to pattern critical transistor source-drain (SD) areas vital to device performance. As device architectures have moved from planar (2D) transistors to 3D Fin Field Effect Transistors (FinFETs) this area has become particularly challenging[3]. Second, there are many types of implant levels each with their own lithographic requirements e.g. SD extension, angled and well implants. In contrast to multiple patterning, implant lithography is now in a state of flux as there is no preferred patterning solution and device makers have adopted a mix and match strategy of exposure wavelength (248nm, 193nm, 193nm immersion) and patterning stack.

In this paper, we will discuss recent trends in implant lithography and demonstrate the key role materials play in addressing key challenges. The first challenge we will cover is how to control reflectivity on advanced substrates with varying topography. In this area, we will discuss the merits of fast etch 248nm and 193nm Bottom Antireflective Coatings (BARCs) as well as ultrathin 248nm BARCs for advanced implant levels. Next, we will discuss the trend towards 193nm immersion lithography for implant levels. In this scenario, cost is a concern and wafer throughput needs to be maximized. We will focus on the development of 193nm immersion implant resists with high dynamic receding contact angle for high throughput and low defectivity. Lastly, we will review the use of Silicon Antireflective Coatings (SiARCs) as hardmasks in trilayer imaging scheme for implant lithography. While this patterning scheme offers superior lithography, the potential for substrate damage using traditional SiARC clean steps is a major concern. We will discuss the development of wet strippable SiARCs which can removed under mild SC1 type conditions.

References

[1] Felch, S.B., Current, M.I. and Taylor, M.C., Proc. NA-PAC 2013, Pasadena, CA, USA.
[2] Radamson, H.H., Zhang, Y., He, X., Cui, H., Li, J., Xiuang, J., Liu, J., Gu, S. and Wang, G., Appl. Sci., 2017, 7(10), 1047, 32pp.
[3] Garner, C.M., Phil. Trans. R. Soc. A., 2012, 370, 4015-4041.

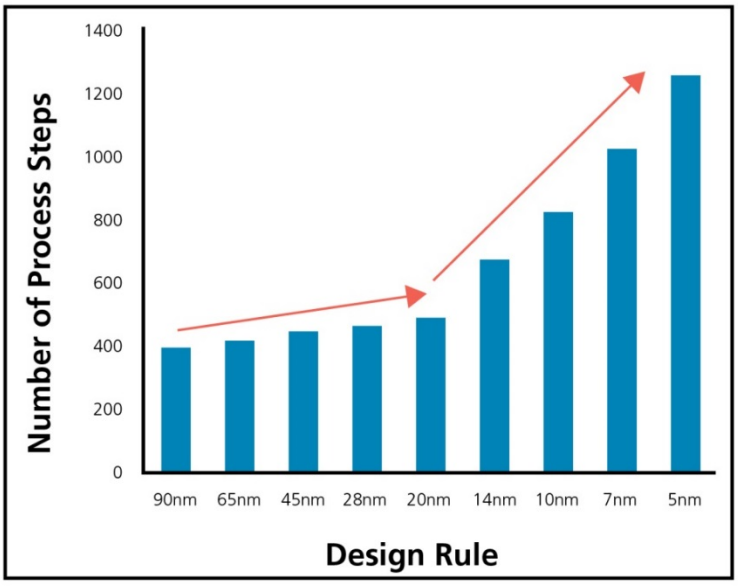

Figure 1. The number of process steps will increase dramatically, starting at 16/14nm nodes. [IC Source: IC Knowledge Strategic Cost Model, KLA-Tencor internal data; Price and Sutherland, "Process Watch: Increasing process steps and the tyranny of numbers," Solid State Technology, July 2015.

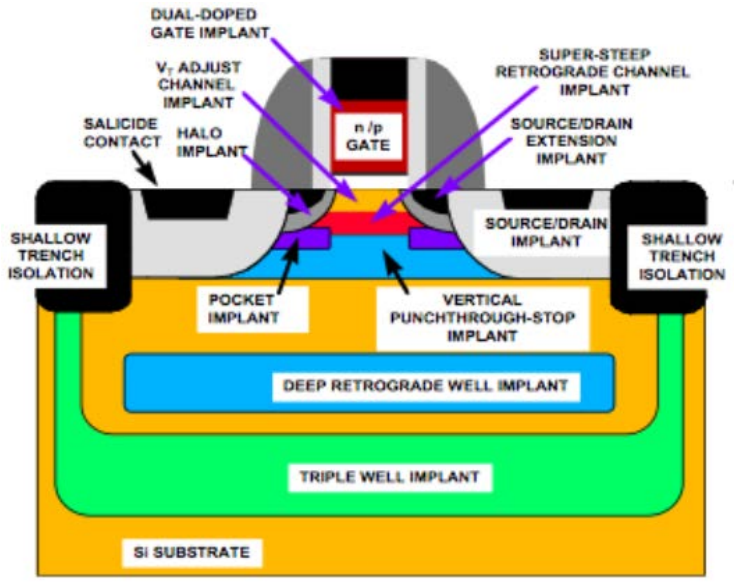

Figure 2: Sketch showing major doped regions for a planar CMOS transistor. Source: [1] Felch, S.B., Current, M.I., and Taylor, M.C., Proc. NA-PAC 2013, Pasadena, CA, USA.