Nano Imprint Lithography for Next Generation Devices

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The biggest value driver in a non-volatile memory was the reduction of bit cost by pattern shrinking with lithography progress. Due to the information explosion, the interest of the market is changing from the bit cost to power saving, latency and long term and huge volume memory applying SSD. The pattern shrinking is reaching a physical limit in device, by the causes of the inter-cell interference, for instance. The device structure is shifting from 2D to 3D. The requirement in lithography for Non-volatile memory device is changing from the higher resolution technology to reduction of process cost such as having higher productivity, manufacturing yield, reliability.

In order to realize low cost memory productions, nano imprint lithography (NIL) technology has aggressively been developing[1)]. Over the past few years, Toshiba, with the support of Canon and DNP, has developed NIL technology for the application of advanced memory devices. We are in the process of verifying the fundamental technologies and the compatibility of NIL to the Si-fab and are now preparing the NIL technology for the production line. To be successful however, we must solve the unique challenges of NIL in defectivity, overlay accuracy, and productivity. Additionally, we have to understand new phenomena in lithography, such as the polymer rearrangement influences on liquid resists, as well as nano-fluidic mechanisms. Potential defect mechanisms such as nano bubble and metal ion content must also be understood and addressed.

Recently, storage class memory called SCM has been a very hot topic in the world, which is expected to fill the gap. SCM will improve system performance for example in latency between DRAM and NAND. Pattern shrinking is restarted in the non-volatile memory again to reduce device cost. However, a new technical challenge in SCM process integration is a thermal problem with semiconductor material. We have to develop low temperature hard mask process with high aspect ratio for SCM pattern shrinking because of material. Lithography challenge for SCM is shown in Fig.1. The multi patterning with spacer process cannot be applied to next generation memory process with ArF immersion and EUVL because of thermal problem for semiconductor material. Low cost single exposure with NIL will be an ideal process. Off course NIL has also many problems in a template fabrication. New template fabrication process has been developed. As show in Fig.2, for next generation memory, the dens patterning of sub-15nm half pitch and beyond on a Si wafer using a template process has been succeeded.

In this paper, the status of the nano imprint lithography for high volume manufacturing is discussed, along with key challenges that must be addressed. Moreover, proprietary technology of NIL such as 3D and wide field patterning is discussed.

References

[1] Tatsuhiko Higashiki, Tetsuro Nakasugi, Ikuo Yoneda, Nanoimprint lithography and future patterning for semiconductor devices, J. Micro/Nanolith. MEMS MOEMS 10(4), 043008 (Oct‑Dec 2011)

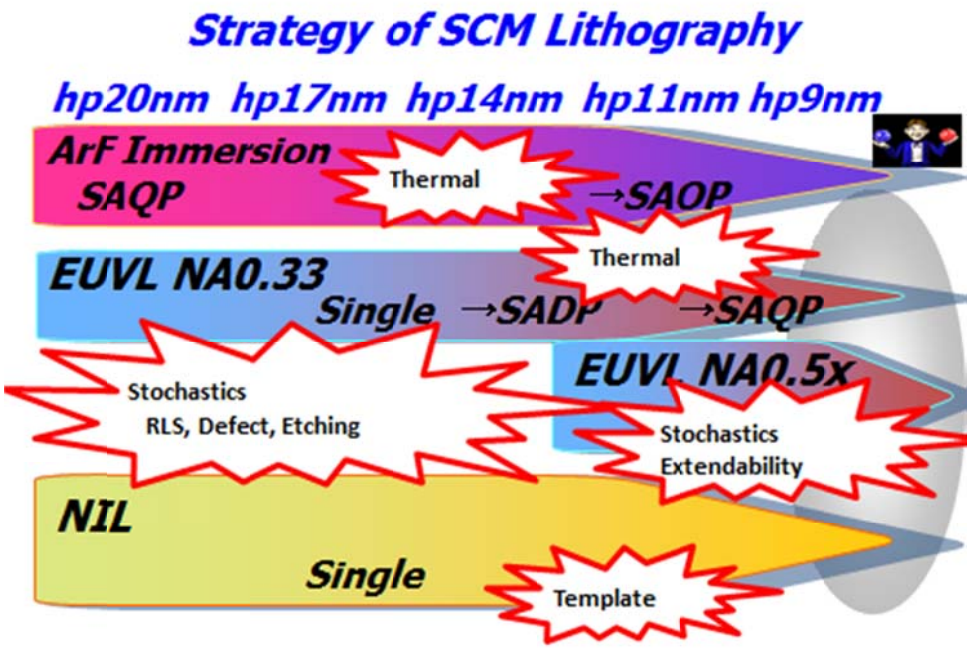

Fig.1 Next lithography challenging

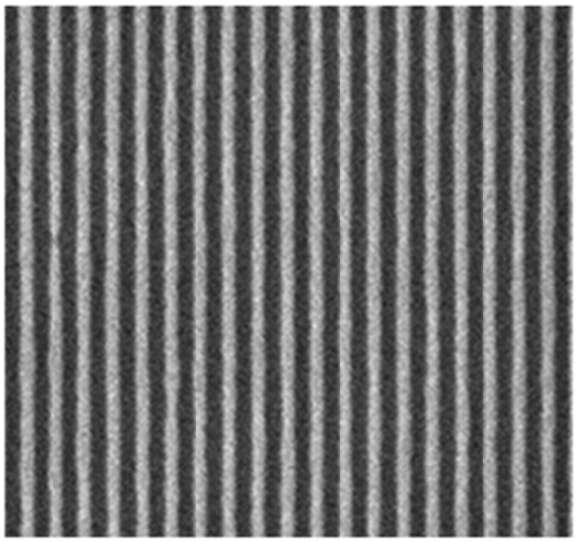

Fig.2 Dens patterning of sub-15nm half pitch and beyond on wafer