Seamless and Scalable Nanofabrication of Silicene Field-Effect Transistors with Prolonged Lifetime

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Two-dimensional (2D) buckled atomic sheets, e.g. silicene and phosphorene, yield collective properties of mechanical flexibility and tunable bandgap in between graphene and transitional metal dichacogenides. Silicene, Si cousin of graphene, is predicted to offer a host of exotic effects, e.g. quantum spin Hall[1], piezomagnetics[2] and thermal electronics[3], for novel nanoelectronics. Nevertheless, there was a lack of experimental device study due to air-stability issue. Our previous work enabled silicene transistor debut[4], corroborating theoretically predicted ambipolar transport with Dirac cone in band structure[5]. Here, we report our continuous effort on further improving portability, fabrication scalability and stability of silicene device.

In this work, we developed a seamless interface process and integrated thermal-release tape delamination transfer to improve portability and reliability in device fabrication. We also discovered that the number of layers also played a role in stabilizing silicene devices. Our new process starts with an *ex-situ* atomic layer deposition (ALD) of 5-15 nm Al_2O_3 on top of *in-situ* Al_2O_3/silicene/Ag/mica stack, followed by 200-300 nm Ag or Au deposition as back gate metal layer (Fig. 1a). Previously, above silicene stack was delaminated from mica first and then subjected to a high vacuum annealing step, significant time (hrs) and energy, to couple with external dielectric and back gate device substrate. The new process not only provides a more reliable interface between back gate dielectric and *in-situ* Al_2O_3/silicene, but also preserves intact silicene (Fig. 2), by forming functional layers of devices beforehand. Besides interface engineering, the delamination transfer step newly employed thermal release tape for better transfer coverage under optimized temperature and surface conditions. Unlike previous process suffering with sub-cm size transfer, this new approach can transfer silicene device stack over a $1 \times ½$ in^2 area with decent uniformity (Fig. 1b), leading to potentially high yield of device fabrication. Electrostatic measurements on fabricated silicene transistors revealed ambipolar electrostatic characteristics in drain current (I_d) response to gate voltage (V_g) with extracted mobility up to 200 cm^2/V-s at residual carrier density $\sim 8 \times 10^9$ cm^{-2} (Fig. 3) proving some theoretical calculations[5, 6]. Although multi-layer silicene transistors show similar, if not better, electrical characteristics as monolayer silicene devices[4], they have notably longer lifetime up to 48 hrs (2 mins for monolayer). It indicates that number of layers is a key knob to tune the stability of silicene devices. This work addresses portability and scalability in silicene device fabrication and device stability, which also sheds light on other air-sensitive 2D Xenes like phosphorene and germanene.

Reference:
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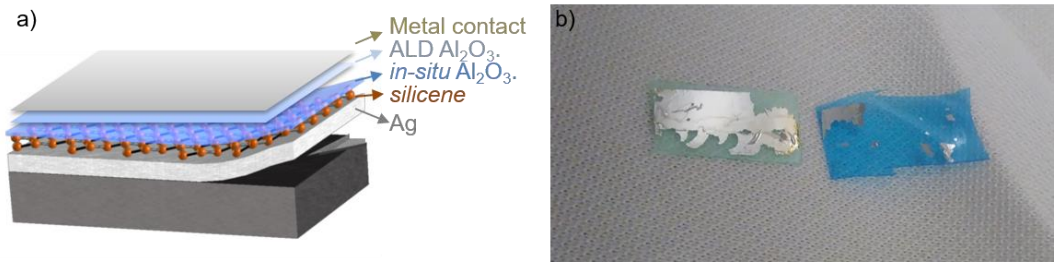

Figure 1. *Silicene device fabrication processes*: **a**) schematics of a seamless integration of back gate metal/*ex-situ* ALD Al_2O_3 with *in-situ* Al_2O_3/silicene/Ag/Mica stack and **b**) large area (0.5 in^2) thermal release transfer of silicene film stack for transistor fabrication.

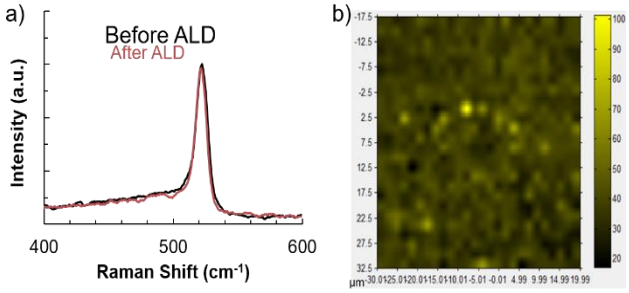

Figure 2: Raman characteristics of silicene: **a**) before and after ALD process showing intact silicene signatures and **b**)50 ×50 μm^2 mapping indicating highly uniform coverage.

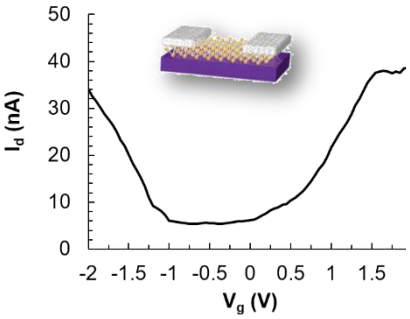

Figure 3. Multilayer silicene device: ambipolar I_d-V_g curve (field-effect mobility ~200 cm^2/V-s and ~10 × gate modulation (stable up to 48hrs).