Highly Parallel Scanning Probe Lithography

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Scanning probe lithography (SPL) in various forms[1-4] has demonstrated significant capabilities including direct deposition of a wide variety of materials[2], thermal ablation of resists to create 3D structures[3], single digit nm lithography[1], and sub-nm digital lithography[4]. However, in most cases these SPL tools and processes are carried out with a single tip, a modest number of probes acting in parallel, or tips in relatively large arrays that have global XY actuation and at best have individual Z axis actuation. This situation and the fact that SPL necessarily is carried out with mechanical scanning, significantly limits the efficiency of the SPL tools and results in patterning throughput that is suitable for research applications but not for scalable manufacturing.

A much more attractive path to SPL which could achieve manufacturing throughput is to go to highly parallel operation of tips that have independent X Y and Z nanopositioning with excellent precision. However, this community has seen the great difficulty encountered while trying to go parallel with e-beam lithography and should be skeptical about any plans to develop highly parallel and highly precise SPL.

On the other hand, it is instructive to examine the problems encountered by parallel e-beam lithography. A major problem is the coulomb interaction of high current density (required for high throughput) beams interacting over the beam paths from source(s) to substrate[5]. While correction for this space charge effect is technically feasible, the scale of the problem increases exponentially as the number of closely spaced high current beamlets increases. There is also the formidable wiring problem and the resulting cross-talk of the many analog signals that must be sent into the beam-blanking/deflection array required to impose the pattern.

The advent of MicroElectro Mechanical Systems (MEMS) based nanopositioning systems[6] allows for closely spaced arrays of tips to be used for SPL. Since the various SPL methods either do not use charged particles, or uses low energy electron beams with very short beam paths which results in negligible coulomb interactions. Further, the problem of running analog control lines into a large array can be avoided entirely by including local CMOS micro-controllers that can receive high-level digital instructions that can be carried out by one or a small cluster of MEMS based SP nanopositioners. A small array of AFMs built entirely in a CMOS foundry has been demonstrated [7]. See Figure 1.

While it would require a non-trivial development effort, we believe that closed-loop XYZ MEMS-based nanopositioners with sub-0.1nm accuracy (challenging but feasible) could be developed and controlled with a local CMOS microcontroller. An array would only require a power bus and a digital address bus dramatically simplifying the integration problem. The nanopositioner (scanner) could receive high level digital commands, carry out the required patterning and inspection and then report back that the pattern was finished and inspected. A global XY positioning system would move the array to cover the entire patterning area.

While there are still some engineering challenges to meet, particularly that of tip robustness that is currently being addressed[8], the path to massively parallel SPL tip arrays is relatively straightforward. We believe that 3 DoF MEMS based scanners could be placed at 200 micrometer X-Y pitches in a 2D array. At that density over 1 million tips could be operated independently, in parallel on a 300mm wafer.

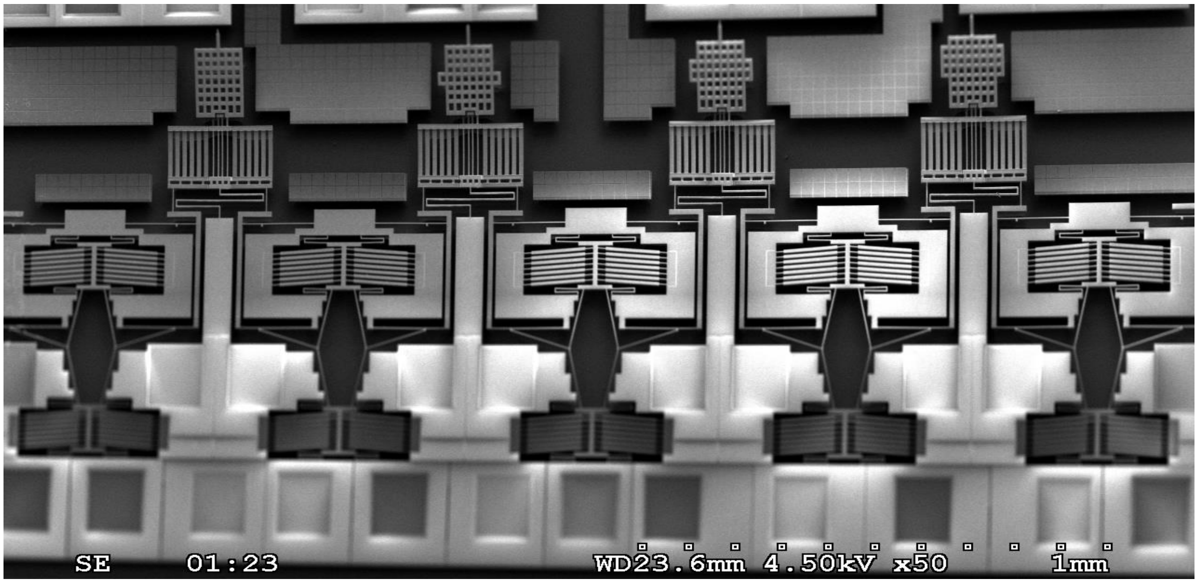

Figure 1: 4x1 array of AFMs on a chip uses "proof-mass-tuning" to separate the natural frequencies of each AFM in the array (Figure courtesy of Integrated Scanning Probe Instruments).

References:

1. Krivoshapkina, Y., Kaestner, M., Lenk, C., Lenk, S., & Rangelow, I. W. (2017). Low-energy electron exposure of ultrathin polymer films with scanning probe lithography. *Microelectronic Engineering*, *177*, 78–86.

2. Ginger, D. S., Zhang, H., & Mirkin, C. A. (2004). The Evolution of Dip-Pen Nanolithography. *Angewandte Chemie - International Edition*, *43*(1), 30–45.

3. Cheong, L.L.; Paul, P.; Holzner, F.; Despont, M.; Coady, D.J.; Hedrick, J.L.; Allen, R.; Knoll, A.W.; Duerig, U. Thermal probe maskless lithography for 27.5 nm half-pitch si technology. Nano Lett. 2013, 13, 4485– 4491.

4. Randall, J. N., Lyding, J. W., Schmucker, S., Von Ehr, J. R., Ballard, J., Saini, R., … Ding, Y. (2009). Atomic precision lithography on Si. *J. Vac. Sci. Technol. B*, *27*(6), 2764–2768.

5. Liddle, J. a., Blakey, M. I., Knurek, C. S., Mkrtchyan, M. M., Novembre, a. E., Ocola, L., … Waskiewicz, W. K. (1998). Space-charge limitations to throughput in projection electron-beam lithography (SCALPEL). *Microelectronic Engineering*, *41–42*, 155–158.

6. Sarkar, N., Mansour, R. R., Patange, O., & Trainor, K. (2011). CMOS-MEMS atomic force microscope. *Transducers 2011*, 2610–2613. http://doi.org/10.1109/TRANSDUCERS.2011.5969836

7. Zyvex Labs - ICSPI report to DARPA on A2P program Jan 15, 2017

8. Tajaddodianfar, F., Moheimani, S. O. R., Owen, J., & Randall, J. N. (2018). On the effect of local barrier height in scanning tunneling microscopy. *Review of Scientific Instruments*, *89*(1), 13701.