The Non-Volatile Redox Transistor for Neuromorphic Computing

A. Alec Talin
Sandia National Laboratory
Livermore, CA 94550

Inspired by the efficiency of the brain, CMOS-based neural architectures and memristors are being developed for pattern recognition and machine learning. However, the volatility, design complexity and high supply voltages for CMOS architectures, and the stochastic and energy-costly switching of memristors complicate the path to achieve the interconnectivity, information density, and energy efficiency of the brain using either approach. In my talk, I will review the latest advances in neuromorphic computing architectures based on deep neural networks implemented using CMOS and memristors and describe the challenges in achieving both high accuracy and energy efficiency using these devices. I will then discuss an alternative approach based on the non-volatile redox transistor (NVRT): a device with a resistance switching mechanism fundamentally different from existing memristors, involving the reversible, electrochemical reduction/oxidation of a material to tune its electronic conductivity. The first type of NVRT that I will describe is based upon the intercalation of Li-ion dopants into a channel of $Li_{1-x}CoO_2$. This Li-ion synaptic transistor for analog computing (LISTA) switches at low voltage (mVs) and energy, displays hundreds of distinct, non-volatile conductance states within a 1V range, and achieves high classification accuracy when implemented in neural network simulations[1]. The second type of NVRT I will describe operates on a similar principle but is based on the polymer system PEDOT:PSS, and which we call the electrochemical neuromorphic organic device (ENODe) [2]. Plastic ENODes are fabricated on flexible substrates enabling the integration of neuromorphic functionality in stretchable electronic systems. Mechanical flexibility makes ENODes compatible with three-dimensional architectures, opening a path towards extreme interconnectivity comparable to the human brain.

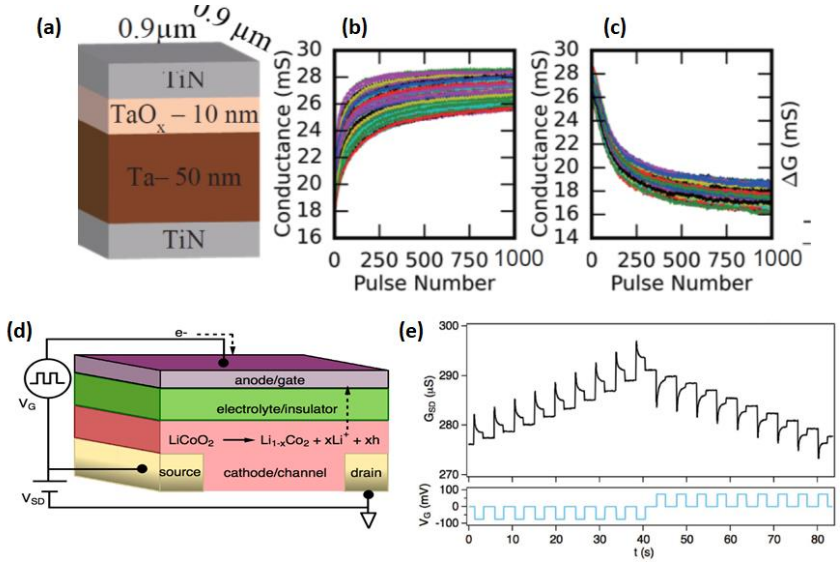

Figure 1 (a) Memristor stack fabricated at SNL (b),(c) conductance states following ±1V pulses for 100 different memristors[3]; (d) Structure of a LISTA, (e) LISTA conductance states following ±0.1V pulses[1].

(1) E. J. Fuller, F. El Gabaly, F. Léonard, S. Agarwal, S. J. Plimpton, R. B. Jacobs-Gedrim, C. D. James, M. J. Marinella and A. A. Talin, Advanced Materials 29, 1604310 2017.
(2) Y. B. van de Burgt, E. Lubberman, E. J. Fuller, S.T. Keene, G. C. Faria, S. Agarwal, M. J. Marinella, A. A. Talin* and A. Salleo*, Nature Materials 16, 414 2017.
(3) S. Agarwal, R. B. Jacobs Gedrim, A. H. Hsia, D. R. Hughart, E. J. Fuller, A. A. Talin, C. D. James, S. J. Plimpton, M. J. Marinella, IEEE 2017 Symposium on VLSI Technology Digest of Technical Papers, DOI: 10.23919/VLSIT.2017.7998164.