Integration of Memristor on CMOS Chips for Hardware Accelerators

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Recent development of high density and low power consumption memristor technology has opened a new door for hardware accelerators in advanced computing. Memristor-based Dot-Product Engine (DPE) and Ternary Content Addressable Memory (TCAM) have shown promising results in applications such as neuro-network computing and network security.[1,2]

Although results are demonstrated from micon size devices, it is important to evaluate the integration of memristor and CMOS at nanoscale. In this paper, we present integration of nanoscale memristor arrays on foundry-built 250 nm CMOS circuit chips with focus on BEoL process and nano device scaling down.

Memristor devices of 20-200 nm are fabricated on 5 mm x 5 mm diced CMOS chips using electron beam lithography. Platinum bottom electrode is formed by e-beam lithography followed by a lift-off process using a double-layer positive e-beam resist. This electrode is connected with the drain of the transistor through a via. A ~5 nm tantalum oxide (TaO_x) is deposited by sputtering as switching layer and selectively etched at the location where a via connects the top electrode and the underlining circuit. The top electrode of tantalum and platinum is fabricated in a similar way to the bottom electrode. Finally, contact pads for probing are formed by photolithography process.

The SEM image in Figure 1 indicates a good alignment of the CMOS and the memristors for a 2x2 TCAM circuit, each contains a 4T2M. Figure 2 shows a device size of ~25 nm at the cross point of top and bottom electrodes. The material stack of such a device can be clearly seen in a cross-section TEM image in Figure 3.

Figure 4 shows the switching characteristics of a 1T1M device with a memristor size of 50 nm x 50 nm at various gate voltages. It is important to notice that at nanometer scale, devices still maintain a high ON/OFF ratio (>100), and the conductance state can also be controlled very well with SET gate voltage. The current and voltage is fully compatible with operation range of CMOS.

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[1] M. Hu, C. E. Graves, C. Li, Y. Li, N. Ge, E. Montgomery, N. Davila, H. Jiang, R. S. Williams, J. J. Yang, Q. Xia, and J.P. Strachan, *Advanced Materials*, 1705914

[2] R. Dhiman, M. Kaur, G. Singh, *Recent Advances in Engineering & Computational Sciences (RAECS) 2015 2nd International Conference*, pp. 1-6, 2015

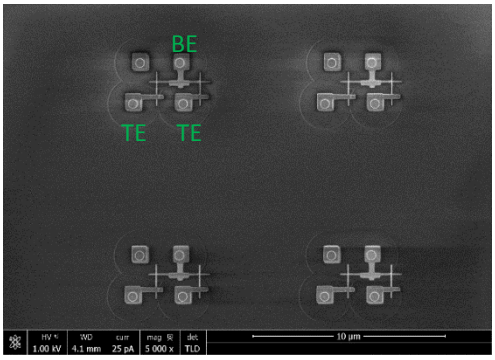

Figure 1: SEM image of a 2X2 TCAM array. The memristor size is about 50 nm X 50 nm.

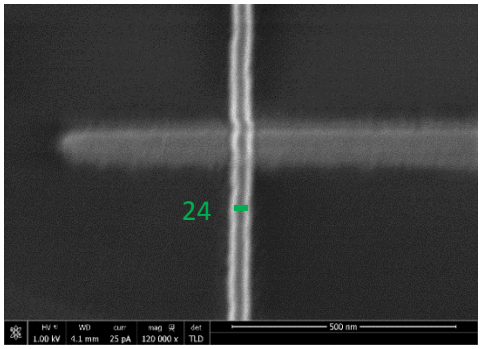

Figure 2: SEM top view of a cross-bar memristor device, scale bar 500 nm.

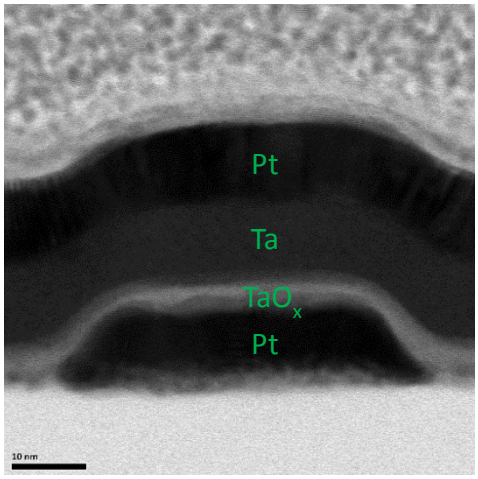

Figure 3: A cross-section TEM image of an ebeam fabricated nanoscale memristor device, scale bar 10 nm.

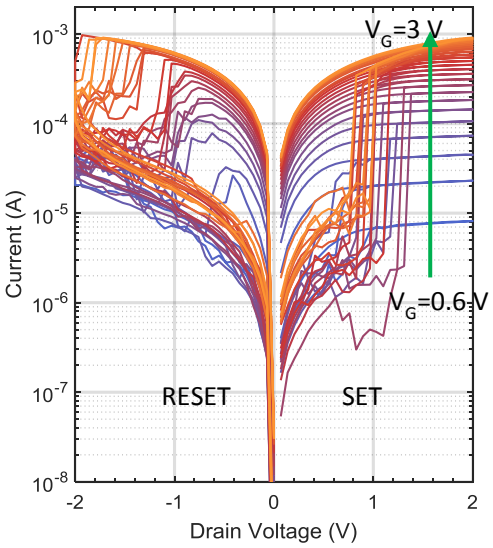

Figure 4: Switching characteristics of a 1T1M device with memristor size of 50 nm x 50 nm at various gate voltages. At a reading voltage of 0.2V, we read the ON state resistance ranging from 150 kOhm to 1.4 kOhm, when memristors were switched on (SET) at gate voltage between 0.6V to 3V.