Fabrication of cryogenic resistors for on-chip shunting of superconducting NbN nanowire devices.

M. Colangelo, E. Toomey, K. K. Berggren
Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, 77 Massachusetts Ave., Cambridge, MA 02139
colang@mit.edu

Recent progresses in thin-film superconducting nanowire electronics and single photon detectors (SNSPDs) have focused on the study of controlling superconducting nanowire dynamics. Toomey *et al*. showed that the use of an external shunt resistor wired bonded to a thin-film niobium nitride nanowire, controls the nanowire heating dynamics by limiting the normal state hotspot expansion. The interaction of the growing hotspot with the external shunt resistor produces high frequency relaxation oscillations, characterized by a time constant proportional to the total inductance of the system; shunting the nanowire externally causes the inductance to be dominated by the contribution of the wire bonds which is difficult to control and replicate. Minimization of the inductance may suppress the hotspot more efficiently, allowing the nanowire to operate using faster, coherent oscillations[1].

In this work we present the fabrication process and preliminary characterization results of lithographically shunted NbN nanowires, featuring on-chip resistors compatible with cryogenic testing temperatures (4.2K) and inductances dictated by nanowire geometry. Figure 1a shows a 30 nm wide shunted NbN nanowire. Thin film NbN (~10 nm) was first reactively sputter deposited on 300nm SiO_2 on Si. The nanowire device and contact pads outlines were defined on GluonLab gL2000M positive resist, by electron beam lithography and then transferred to the NbN by CF4 reactive ion etching. In order to avoid shorting the resistor with underlying NbN, a window was created by first patterning Shipley S1813 positive resist with aligned direct writing photolithography, and then etching the NbN. Afterwards, resistors were defined over the window by a second aligned direct writing photolithography on a s1813/PMGI bilayer resist stack, engineered to obtain an undercut (Figure 2) and favoring flat metal profiles after lift-off. A ~20nm Ti layer was sputtered and lifted off in 40 °C NMP. We also demonstrated a slightly modified process, avoiding one step of aligned photolithography and using evaporated 35nm Ti/5nm Au, which was used to fabricate a 3 μm x 4 μm 80 nm wide shunted SNSPD from ~7nm thick NbN (Figure 1b).

Resistive metallic layers were characterized versus temperature showing a stable resistive state at 4.2K, thus qualifying for cryogenic use. Current-voltage characterization showed a fully suppressed hysteresis (Figure 3a), confirming effective control of heating dynamics control by local lithographic shunting. The absolute reduction of total system inductance also allowed fast relaxation oscillation in highly inductive SNSPD devices (Figure 3b) creating room for novel coherent applications. Use of these high speed oscillations as frequency-based sensors is currently being investigated.

[1]Toomey, E., arXiv preprint arXiv:1709.06598, 2017

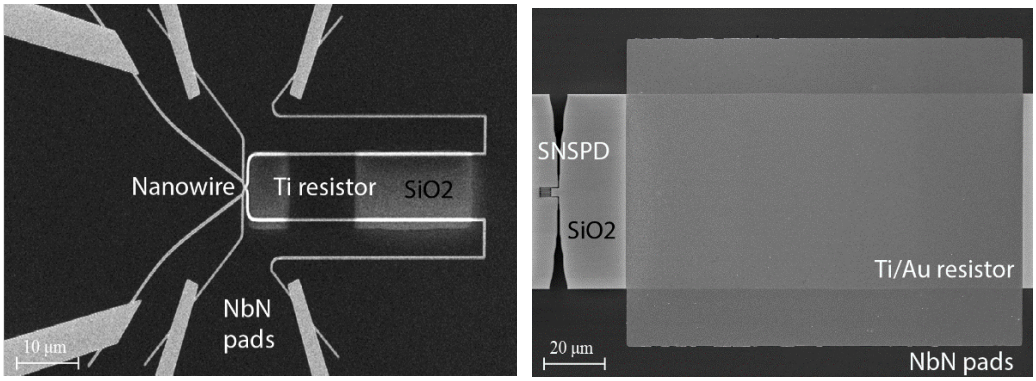

Figure 1: a) SEM micrograph of a 30 nm NbN nanowire shunted with a sputtered Ti resistor; b) SEM micrograph of of a 3 µm x 4 µm 80 nm wide NbN SNSPD shunted with an evaporated Ti/Au resistor

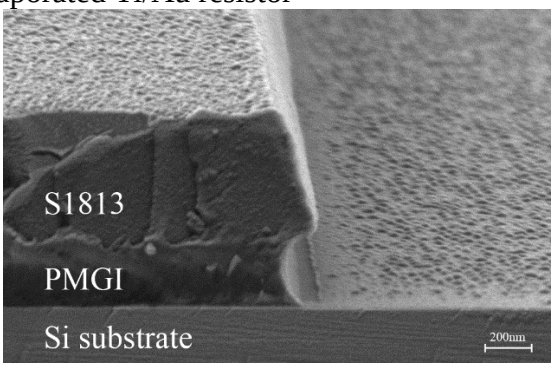

Figure 2: Cross section SEM micrograph of a test chip showing bilayer resist (S1813+PMGI) undercut obtained after development. This process has been applied to obtain flat metal profiles after lift-off.

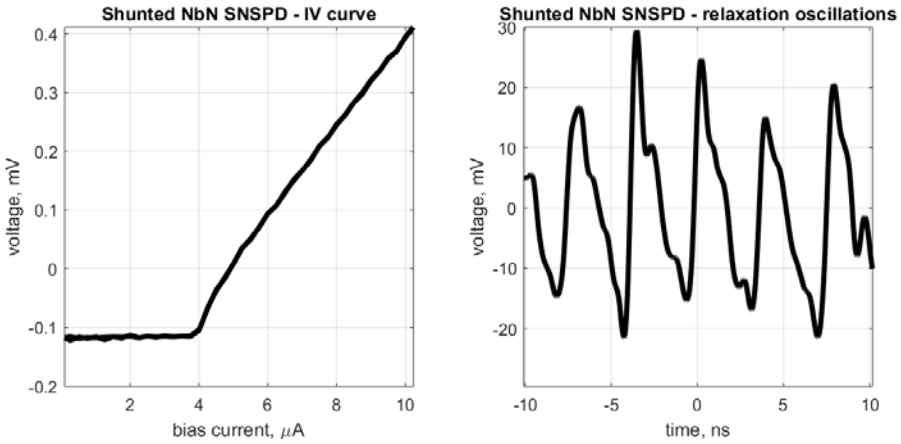

Figure 3: Characterization of shunted SNSPD of Figure 1b: a) non hysteretic current-voltage curve confirming the controlled Joule heating state achieved by shunting; b) waveform of the relaxation oscillations induced by the interaction of growing hotspot with external shunt resistor