Patterning of Dense Arrays for MRAM Applications

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MRAM is gaining traction as a high performance embedded memory replacement for eFlash, eDRAM, and even eSRAM. For standalone memory chips, MRAM is the only emerging NVM technology capable of approaching DRAM performance. If it is to be widely adopted for anything other than niche standalone applications, however, the density of MRAM must approach that of DRAM, which means much tighter pitches than those being commercialized for embedded applications.

STT-MRAM has approximately 20 metallic layers, many of which are incompatible with RIE. As a consequence, ion beam etch/milling (IBE) has been adopted as the primary etching technology for MRAM. To assess the feasibility of a tight array fabrication processing for MRAM, we used e-beam lithography to pattern a matrix of arrays in 30 nm thick HSQ resist. The full pitch of the arrays ranged from 200 nm to 65 nm and the corresponding dot sizes were from 100 nm down to 20 nm in diameter. By using the HSQ dot as the hard mask (HM), the array pattern was transferred to a Cr 8nm/TaN 75nm HM stack via two reactive ion etch (RIE) steps. This hardmask was subsequently used to ion mill the MRAM stack to its base.

With the 75 nm TaN hardmask, we have fabricated MRAM device arrays with a full pitch down to 65 nm, and electronic transport measurements show no degradation of the MRAM bit performance. Shadowing effects during the milling process limit the ultimate pitch we can obtain with that technology. To extend the full pitch below 65nm, we have recently developed a shorter composite HM stack with superior milling selectivity, and achieved physical separation without re-deposition at 55 nm full pitch, which is on par with current DRAM densities.