# Advance Lithography I-Line Resist Profile for Difficult Liftoffs in Compound Semiconductor Technologies

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Compound semiconductor devices commonly rely on gold as the basis of their source and drain process modules. Due to the inherent chemical stability of gold, the patterning of these features has relied on liftoff techniques compared to the subtractive/etching processes used in silicon and CMOS based fabrication.

The compound industry standard for photoresist (PR) liftoff profiles patterned in I-line/DUV can be described in two distinct methods. In the first method, a bilayer process uses a standard resist profile over a soluble sacrificial liftoff resist (LOR) that etches isotopically during the resist development process, creating an undercut profile suitable for metal liftoff. (Fig. 1A) The disadvantage of this resist profile during the metal deposition process is that the metal film stack is evaporated onto the top of the resist and a small fraction of the metal stack is also deposited on the sidewalls of the photoresist. (Fig 1B) If the top resist sidewall profiles are < 90° due to imaging processing shifts, the side wall metal is coated thicker causing the liftoff to become even more difficult to remove. In this scenario, when the metal deposits thicker on the side walls of the resist, the metal sidewall debris can remain in the source drain channel after the lift off step, interfering with the imaging of the gate process or forming an electrical short to the gate. The second method uses a single-layer positive resist process with the top of the resist chemically modified to create an inhibition layer used during the resist development process, resulting in an overhang or lip profile. (Fig 2A) The overhang profile helps to shadow the sidewall wall during the metal deposition process, but due to the angle of evaporation or throw of the evaporation system, the metal may be deposited off center from the resist trench. This causes the metal to accumulate onto the outer most side walls of the outer row and columns of a wafer, resulting in metal tears or wings coming from the metal and substrate interface. (Fig. 2B) Additionally, since this metallization may occur on or close to a regrown contact for certain devices, the non-planar surfaces result in additional complexity as opposed to planar surfaces.

To overcome these challenges, this work demonstrates a process that combines both of the above mentioned techniques to create a resist profile with a top lip over a bi layer. (Fig.3A) Such a profile has been created using a combination of develop pre-soaks and post exposure bakes. This profile mitigates many of the drawbacks mentioned earlier. Fig. 3B shows metal deposited on such a PR profile where a clean break is still observed. To highlight the robustness of this process, this pattern is also demonstrated on a non-planar surface as may be required in compound semiconductors for source drain patterning.

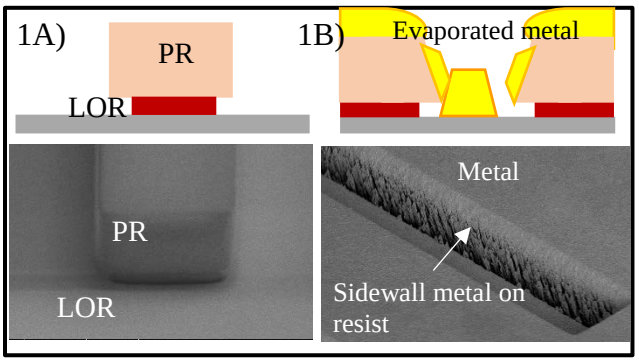


Figure 1: A) Bi-layer resist profile with either LOL/LOR creating an undercut. B) Post metal evaporation and before liftoff. Example of worst case scenario where metal is coated on resist sidewall and connects with metal underneath. This has the potential to leave behind wings post liftoff.

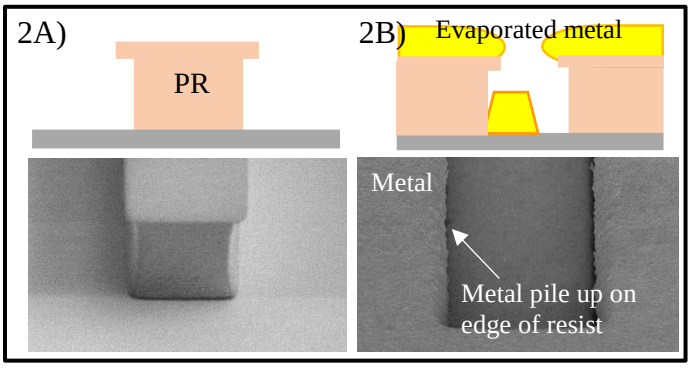


Figure 2: A) Resist profile with top lip. B) Post metal evaporation but before liftoff. Example of worst case scenario where deposition is off centered resulting in a metal pile up on edges of resist

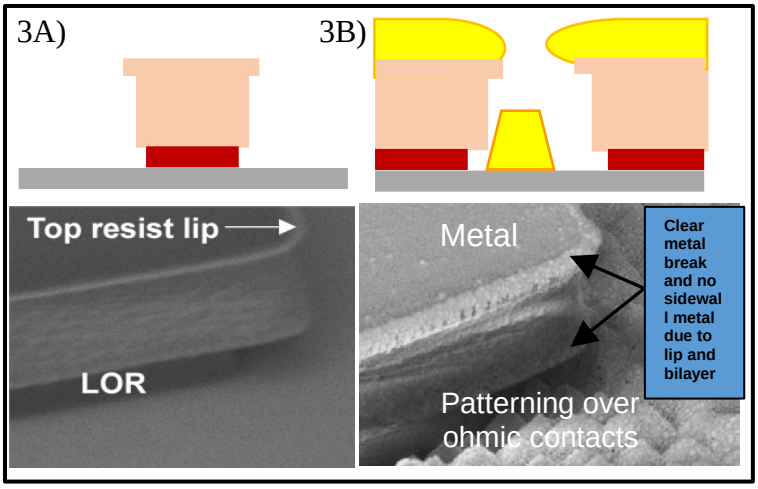


Figure 3: A) Resist profile that has combined bi-layer with top lip. B) Post metal deposition. This patterning is over a non-planar surface showing worst case scenario, but still demonstrating a clear break.