Etching Process for Producing Variable Sloping Sidewall of III-V Antimonide-based Materials for LED/PD Applications

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To satisfy the rapid growth requirement for mass produced ultra-low power consumption gas sensors, particularly using III-V antimonide epi-grown narrow bandgap structures to produce compound semiconductor light emitting diode (LED) and photodiode detector (PD) through development of novel mid infrared (MIR) edge emitting LED and PD devices, a reliable and controllable etching process through mask engineering and inductively coupled plasma (ICP) etching of the III-V antimonides has been explored in this work to obtain a smooth and sloping sidewall etching profile of Al(Ga)InSb based semiconductor materials which is a key step to make the edge emitting LED and PD devices. [1]

The III-V antimonide device materials were grown in Molecular Beam Epitaxy (MBE) method with desired quantum well narrow bandgap layer structure based on variable AlInSb, InGaSb, AlGaSb, and InGaAlSb compound semiconductor compositions. Etching was carried out using an Oxford Instrument PlasmaLab Inductively Coupled Plasma (ICP) etching system with Shipley resist and SiN film deposited by ICP chemical vapor deposition at room temperature as mask.

In the experiments, various gas compositions of CH_4, H_2, Ar, and $SiCl_4$ under various plasma conditions have been used to get controllable sloping profile, which showed some difficulties if using resist as etching mask. A high etching temperature, up to 260ºC, is required for etching indium contained materials in this case but also brings some problems to the resist mask particularly when deeply etching III-V antimonide along with a controllable sloping profile. SiN has been used as etching mask material to address the problems. SiN can be easily patterned to form a sloping profile usable for etching the antimonides from a reflowing resist mask as shown in Figure 1. Various methods have been used to get a desirable SiN mask profile, in which varying the SiN etching condition would be another reliable way as shown in Figure 2, where the III-V antimonide materials have been etched under same etching conditions but SiN etching masks obtained from different SiN etching conditions. In this way, processing has been focused on an easily controlled etch condition. Therefore, a well controlled and reliable etching process has been successfully developed and is being used for fabricating the edge emitting LED and PD devices for gas sensor applications.

[1] A. ROGALSKI, Opto−Electron. Rev. **20**(3), 279 (2012).

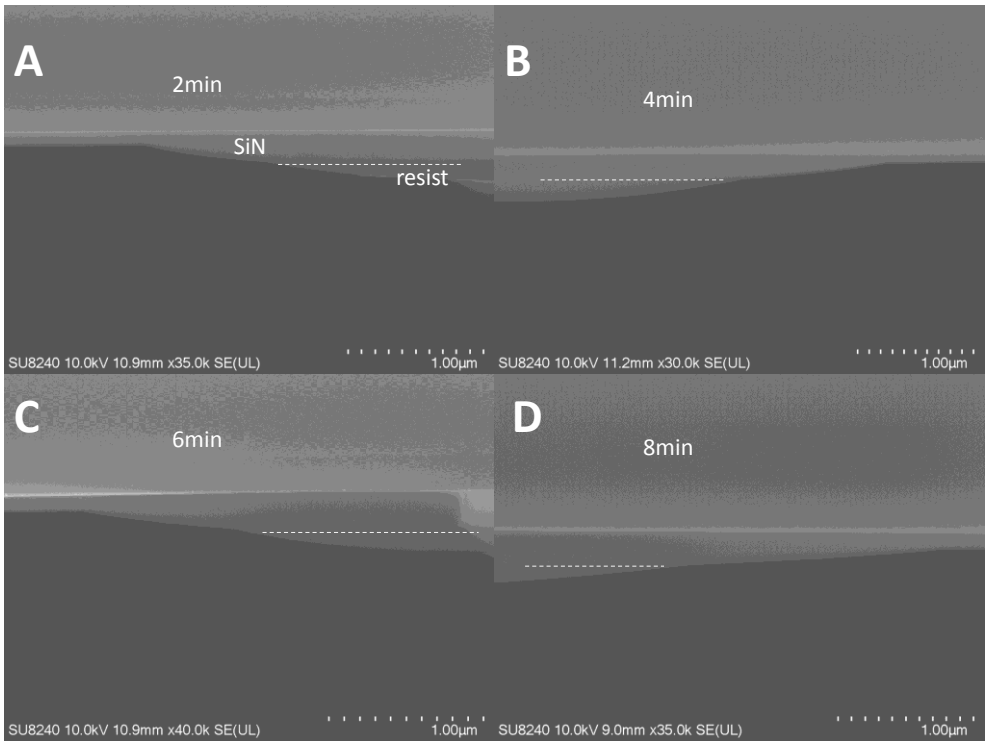

Figure 1: SEM images show effects of resist post-baking time at 180°C on SiN etching profiles, where the sloping angles of the resist and the etched SiN decrease along with the baking time increasing, where SiN etched in chemistry of SF_6:O_2:N_2 = 5:4:51 (sccm) with RF power 50W only at 10ºC and 10 mTorr.

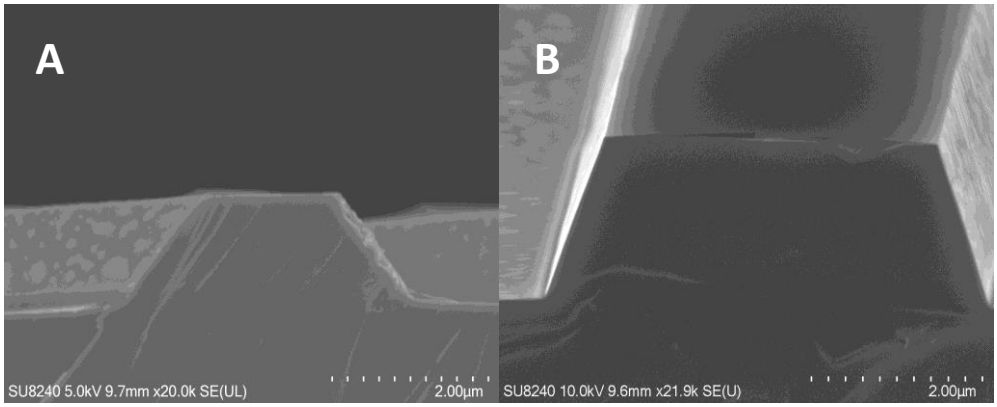

Figure 2: SEM images of etched Al(Ga)InSb profiles from (A) a ~45º slope obtained by etching at 120°C for 23mins with CH_4:H_2:Ar:$SiCl_4$ = 15:50:5:5 (sccm), ICP power 750W, RF power 150W, pressure 15mTorr and etching mask formed via resist S1805 post-baking for 8mins in a 180ºC oven, followed by 200nm SiN etching for 7mins 35secs plus 30secs over-etch at 10ºC and 10mTorr in gases SF_6:O_2:N_2 = 5:4:51 (sccm) with RF power 50W only and then a pre-etch O_2 plasma clean for 4mins with O_2 = 50sccm at 10ºC and 20mTorr with ICP power 2000W and RF power 50W and (B) a ~75° slope under the same etching conditions as (A) except a difference in mask formation (SiN etched at 40ºC).