

# **Fabricating multilayer channel by double nanoimprint lithography**

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The multilayer channel has many applications due to its microstructure. On the microscopic level, this channel can be used as a site in chemical reaction [1], and the nanoscale multi-layer channel can be used as macromolecular screening and the gas-liquid mass transfer [2] But it is difficult to fabricate multi-layer channel by traditional technology due to its focus issues. Recently, double nanoimprint lithography was introduced to fabricate new structure and reduce the feature size [3]. In this paper, the multilayer channel was fabricated by double nanoimprint lithography with the low-cost.

Fig. 1 shows a schematic illustration of the fabrication process for multilayer channel. The 20mg/ml Poly(3-hexylthiophene-2,5-diyl) (P3HT) in 1,2-Dichlorobenzene was spin-coated on the silicon wafer. After that, the 300nm width with 300nm depth polymer gratings was fabricated by nanoimprint at 150 °C with a pressure of 100N/cm<sup>2</sup>. Because the P3HT is a polymer, we choose oxygen as the etching gas to remove the unwanted residual layer. Then the pattern was transferred to silicon substrate by ICP-RIE etching, the depth is 100nm. After the first imprint, we used the grating molds with 5μm width and 100nm depth to make the second imprint. Then we also used ICP to etch 70nm depth silicon. The distance between the first channels is 167.0nm, and the distance between the second channels is 46.5nm, shown in figure 2.

[1] Y.H. Mori, T.G.M. van de Ven, S.G. Mason. Resistance to spreading of liquids by sharp edged microsteps. *Colloids and Surfaces*, Volume 4, Issue 1, January 1982, Pages 1-15;

[2] X Qiu et al 2017 *J. Micromech. Microeng.* 27 047001;

[3] Xiaohao Ma, Dandan Deng, Dehu Cui. Double nanoimprint lithography: A technology for effectively reducing feature size. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* 35, 06G304 (2017);

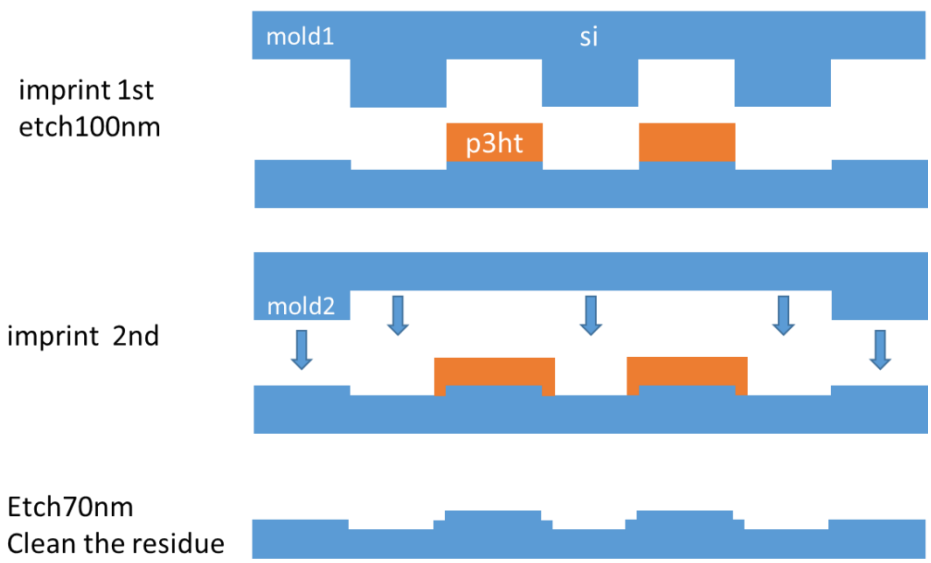


Figure 1: The schematic for fabricating nano-steps.

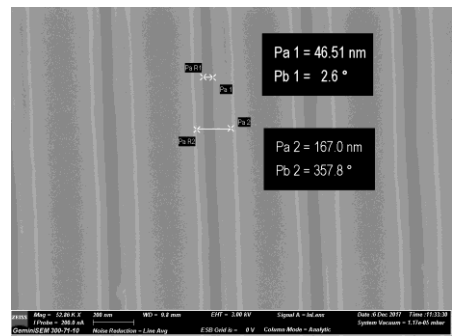
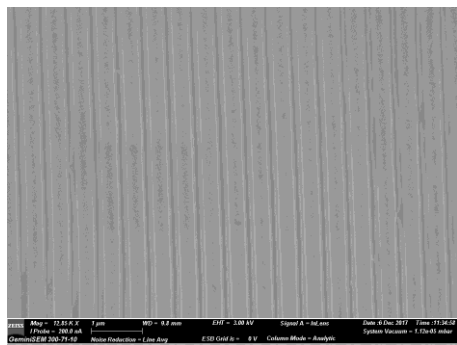


Figure 2: The nano-step structures.