

# High-aspect-ratio gold electroplating for microelectronic, optoelectronic, and microsystem applications

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High-aspect-ratio electrodeposition of gold is a key technology in fabrication of microelectronic, optoelectronic and microsystem devices<sup>1</sup>, and various imaging applications from x-ray optics<sup>2</sup> to biosensors<sup>3</sup>. Fabrication typically involves creating a high-aspect-ratio mold and then filling the trenches with gold by electroplating. Gold deposit should be ductile, low stress, fine grain and void-free. Uniform void-free electroplating of very high-aspect-ratio submicron trenches is a challenge. Two electroplating techniques have been described in the literature: plating from bottom up using a seed layer prior deposited on the wafer bottom<sup>4</sup>, and a full-surface plating, when seed layer is deposited on all surfaces before electroplating<sup>5</sup>. The second method has an advantage of much shorter electroplating time, but it is challenging to avoid prematurely sealing the trenches achieving uniform plating over the entire trench depth and entire plating area. Despite many publications, there is a lack of detailed information on how to achieve a reliable gold electrodeposition into sub-micron wide and tens-micron high trenches, especially over a large plating area.

In the present study, we report gold electrodeposition into high-aspect-ratio nanometer-wide trenches. Two different commercially available non-toxic sulfite-based gold electroplating solutions were used. Two electroplating techniques, bottom-up and full-surface electroplating, were used to fill the trenches. A uniform void-free filling of high-aspect ratio sub-micron silicon gratings (Figure 1) and nanoporous anodic aluminum oxide (AAO) membranes (Figure 2) have been reliably achieved.

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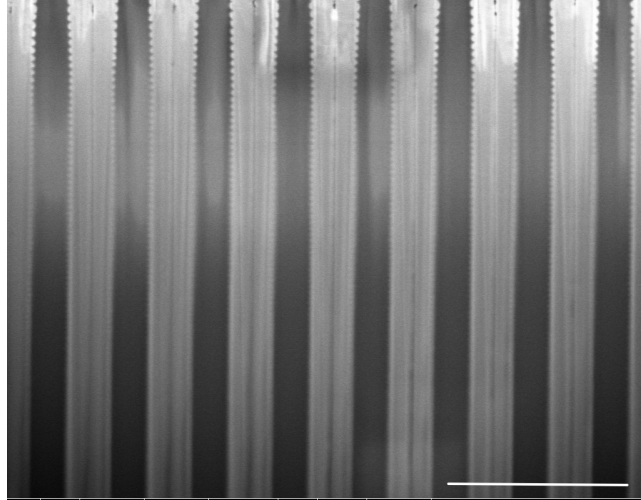
<sup>1</sup>T.A. Green. *Gold Bulletin*. 2007, 40/2, 105-114. <https://doi.org/10.1007/BF03215566>

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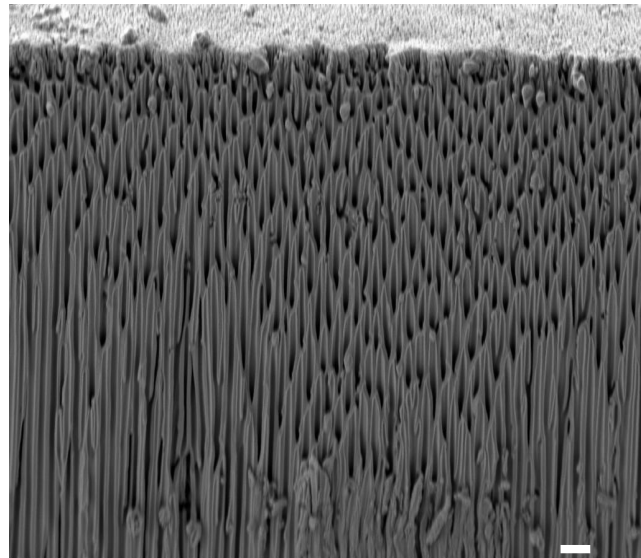
<sup>3</sup>J. McPhillips, A. Murphy, M.P. Jonsson, W.R. Hendren, R. Atkinson, F. Höök, A.V. Zayats and R.J. Pollard. *ACS Nano*, 2010, 4 (4), pp 2210–2216. <http://dx.doi.org/10.1021/nn9015828>

<sup>4</sup>D. C, Bruder J, Rohbeck T, Grunzweig C, Kottler C, Diaz A, Bunk O, Pfeiffer F. *Microelectronic Engineering*. 2007;84:1172–1177. <http://dx.doi.org/10.1016/j.mee.2007.01.151>

<sup>5</sup>S. Znati, N. Chedid, H. Miao, L. Chen, E.E. Bennett, H. Wen. *J. Surface Engineered Materials and Advanced Technology*, 2015, 5, 207-213. <http://dx.doi.org/10.4236/jsemat.2015.54022>



*Figure 1:* Scanning electron microscopy (SEM) cross-section image of an array of 650 nm wide and 14  $\mu\text{m}$  deep trenches in silicon uniformly electroplated with gold using full-surface plating technique (scale bar represents 3  $\mu\text{m}$ ).



*Figure 2:* SEM image of 20 nm Au nanowires grown in an AAO template: height is 60  $\mu\text{m}$  using bottom-up plating technique (scale bar represents 1  $\mu\text{m}$ )

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