Effects of Crystallinity of Switching Layer Material on Memristive Device

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Recently, the development of ReRAM (*i.e.* memristor) [1] has attracted great interest among the semiconductor industry. Significant progresses have been made in memristive device development, including its integration with Si CMOS circuit, switching cycles up to 10^{12}, switching speed down to 100 ps and retention time up to a few years. So far, most efforts are targeting at high-density non-volatile memory applications. There are also many other emerging applications that can greatly benefit from memristors. For example, the memristors can be used as reconfigurable interconnect to save area and power. However, the reconfigurable interconnect has various requirements, such as device resistance, device linearity, size scaling, switching speed and operation voltage. Therefore, significant effort is still needed to tailor the existing memristor technologies for reconfigurable interconnect. Except the traditional method by selecting appropriate material as the oxide and contact layers, we demonstrated a new method to optimize the memristor performance specifically by controlling the crystallinity of the switching layer material.

Figure 1 (a) and (b) show the schematic diagram and optical microscope photo of memristive device. To achieve high linearity required by the reconfigurable interconnect application, the Tantalum (Ta) layer is inserted between top electrode layer and switching layer. After the selection of different switching layer material, Al_2O_3 is proved as a promising switching layer material. Then, the Atomic Layer Deposition (ALD) is chosen to deposit switching layer. This not only ensure the fabrication repeatability and the possibility of scale up for mass production, but this also could decide the crystalline of the switching layer (Al_2O_3) by controlling the deposition temperature. Figure 1 (c) and (d) show the XRD spectrum of Al_2O_3 film deposited at 80 ℃ and 200 ℃ using ALD, which demonstrate the crystalline of Al_2O_3 switching layer can be decided through controlling deposition temperature.

Device resistance and operation voltage of memristive device have a large effect on the application for reconfigurable interconnect. Comparing Figure 2 (a) and (b), the difference (On/Off ratio and operation voltage) of memristive devices is large. These results demonstrate that the performance of memristive device could be optimized specifically through adjusting the switching layer growth conditions.

Switching speed, endurance and variation are all important parameters. As shown in Figure 3, after choosing appropriate Al_2O_3 crystalline and switching layer thickness, the memresitive device can be switched continuously by pulses. The endurance ($\geq 10^3$) and variation also satisfied the requirement of reconfigurable interconnect. Besides, this is also a forming-free memsitor, which is very important and useful for reconfigurable interconnect.

Reference:
[1] Strukov, D.B., et al., *The missing memristor found.* Nature, 2008. **453**(71 80-83.91): p.

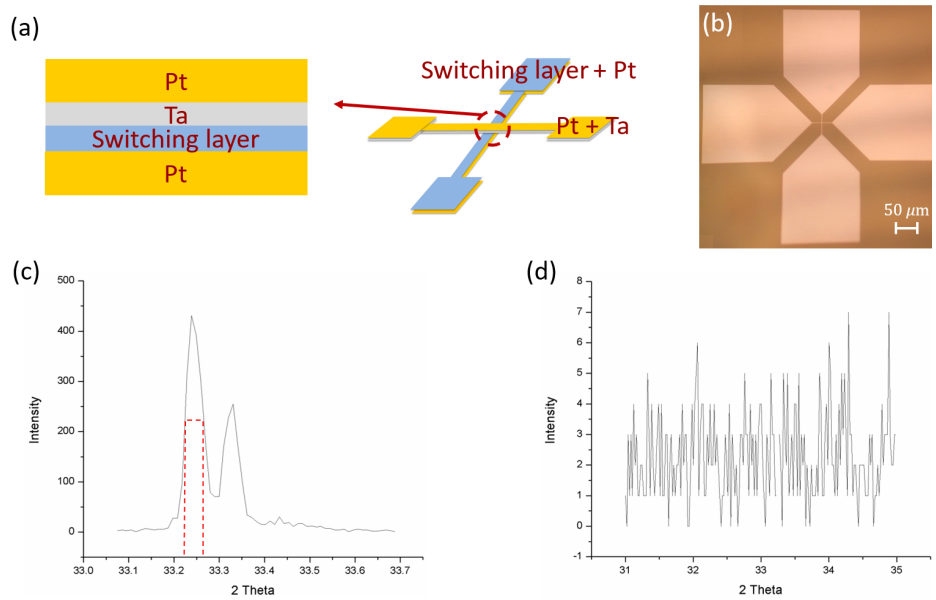

Figure 1: (a) Schematic diagram of memristive crossbar device, which has a four layers structure. (b) Optical microscope photo of $2\mu m * 2\mu m$ memristive crossbar device. (c) XRD pattern of 200 ℃ deposited Al_2O_3 (polycrystalline) film. (d) XRD pattern of 80 ℃ deposited Al_2O_3 (amorphous) film.

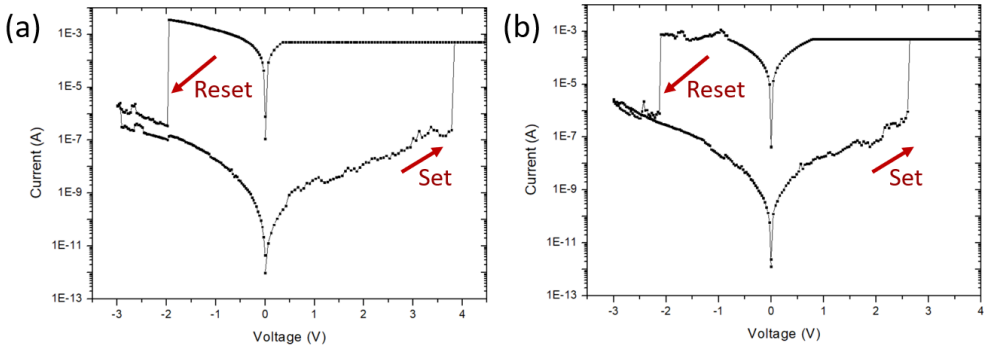

Figure 2: (a) I-V switching curve of 20nm Pt/8nm 200 ℃ deposited Al_2O_3/8nm Ta/20nm Pt memristive device. (b) I-V switching curve of 20nm Pt/8nm 80 ℃ deposited Al_2O_3/8nm Ta/20nm Pt memristive device.

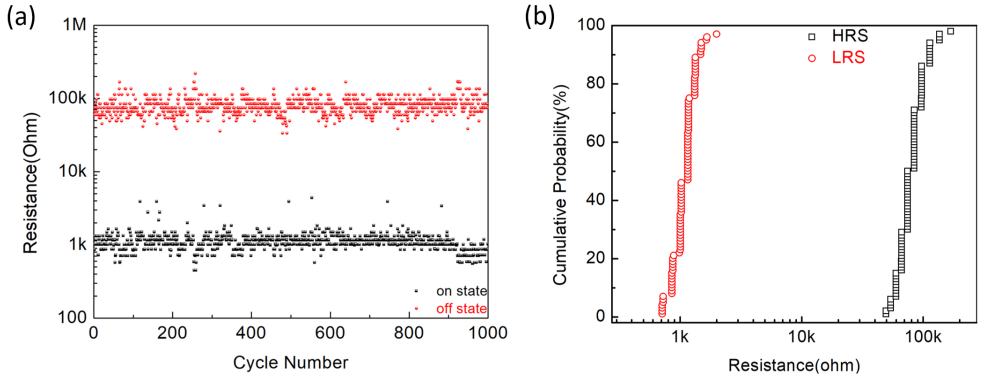

Figure 3: (a) For 20nm Pt/4nm 80 ℃ deposited Al_2O_3/8nm Ta/20nm Pt device, 1000 cycles have been demonstrated with set pulse of 2.3V, 3 μs and reset pulse of voltage -2.6V, 0.4 μs. (b) Resistance distribution of at HRS and LRS in (a).