The Importance of High-Level Simulation in the Co-Design of Neuromorphic Systems

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Neuromorphic computing systems (NCS) are becoming increasingly popular in the beyond Moore's law computing landscape. A wide variety of nanodevices have been studied for NCS, such as metal oxide memristors[1] and carbon nanotubes[2], and are typically used to implement synapses and/or neurons. A key issue associated with most work in this space is that low-level functionality is demonstrated, but implications of that low-level functionality for real applications are not examined. For example, many synapse implementations demonstrate some form of spike-timing dependent plasticity (STDP), a learning mechanism, but the precise functionality of STDP is different from system to system. Differences in STDP affect high-level functionality, but the precise impact on performance is not clear. In general, understanding the impact of low-level functionality on high-level performance will be vital for developing and tuning devices moving forward. Our team and collaborators are exploring the development of and use cases of a variety of neuromorphic devices, including metal oxide memristors and biomolecular memristors. These devices are highly tunable through a variety of mechanisms. To understand the effect of these tunable characteristics on higher level performance, we connect low-level device modeling with high-level simulations that allow for understanding the impact of device behavior on real application performance. These simulators exist in a greater software framework that allows for training on existing applications, including control and classification tasks. This software framework has successfully demonstrated the ability to explore metal-oxide memristor implementation of synapses[3]. This framework allows us to examine the effects of device tuning on application performance and will allow us to understand how to build and tune better devices in the future.

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[3] Plank, J. S., Rose, G. S., Dean, M. E., Schuman, C. D., & Cady, N. C. (2017, November). A Unified Hardware/Software Co-Design Framework for Neuromorphic Computing Devices and Applications [Online]. *IEEE International Conference on Rebooting Computing (ICRC 2017)*: http://ieeexplore.ieee.org/document/8123655/