Fabrication Capabilities for Superconducting Quits at MIT Lincoln Laboratory

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The superconducting qubit modality is receiving a lot of attention from industry and academia as efforts continue to push the boundaries of quantum computing. Complex superconducting circuits can be fabricated using integrated-circuit processing techniques and the properties of these circuits can be purposefully designed and controlled. A key metric for the performance of these devices is the qubit's coherence time, which has been steadily rising with advances in design and fabrication.

MIT Lincoln Laboratory is working to increase addressability and connectivity of our high coherence qubit circuits with 3D integration techniques. We are developing a three-tier stack process that separately fabricates qubit, interposer, and readout/interconnect chips. These are then connected with In bump bonding and through-Si vias, as shown in Figure 1. This process utilizes hard stop Si mesas to precisely control stacked chip spacing, In bump bonding to connect ground planes and carry current between stacked chips, and air bridge crossovers and through-Si vias to enable compact signal routing and more. I will discuss the fabrication and integration of some of these key features and their impact on device performance.

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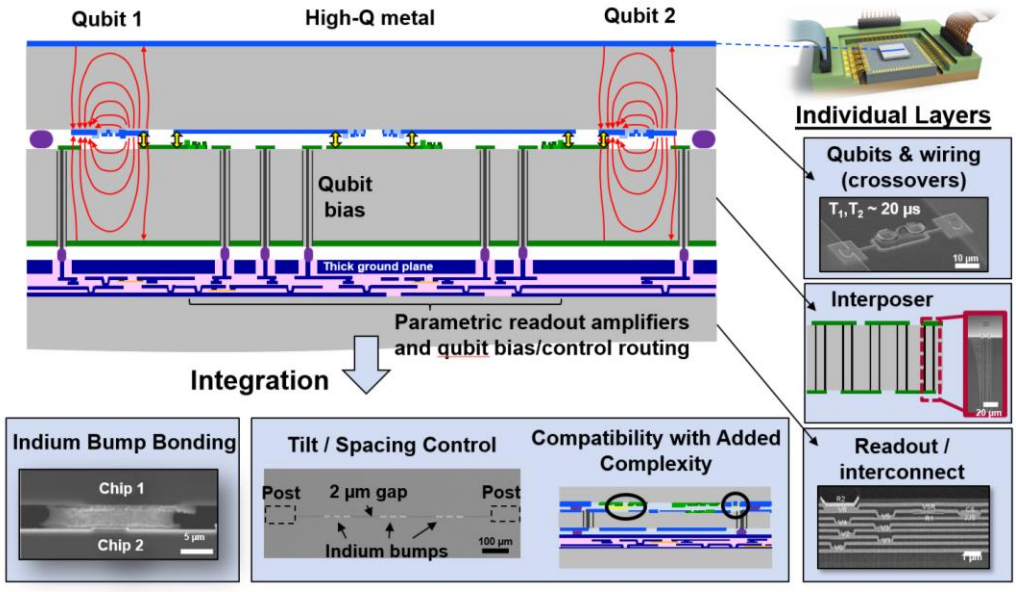

Figure 1: MIT Lincoln Laboratory Three-Tier Stack Qubit Design: The Lincoln three-tier stack architecture uses 3D integration techniques to electrically couple three separately fabricated chips. The fabrication features of hard-stop Si mesas, superconducting air bridges, superconducting through-Silicon vias, and In bump bonding enable complex qubit designs without sacrificing performance.