Cs Ion Coldbeam Suitability for Circuit Edit and Additional Nanomachining Applications

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Focused Ion Beams (FIBs) have been widely used as nano-machining tools in semi-conductor applications such as Circuit Edit and Transmission Electron Microscopy (TEM) lamella preparation. These applications have been enabled for the last three decades by Ga LMIS (Liquid Metal Ion Source) FIB technology. Biennial shrinkage of device dimensions in chip manufacturing, aka Moore's Law, has driven a resolution improvement requirement exceeding √2 for FIB tools. Recently, however, Circuit Edit has been losing critical performance capability on chip manufacturing technologies, such as Intel's 10nm and 7nm processes. The areas of capability loss are primarily in milling acuity, image resolution and the signal to noise ratio (SNR) of the secondary electron (SE) image generated by the FIB, and used for milling alignment and endpoint.

In the present advent of novel FIB source technologies, we have been assessing FIB candidates with significantly improved performance over Ga LMIS FIBs for Circuit Edit performance, and potential for other applications. Performance improvements are primarily in beam resolution, and in some cases improved SE image SNR. New FIB source technologies suited for nano-machining include GFIS (gas field ionization source) with Ne or N_2 ions, and laser-cooled atom ion sources, aka "coldbeams" with, among others, Cs and Rb ions.

We performed extensive testing on the Low Temperature Ion Source (LoTIS) at zeroK Nanotech – a Cs cold ion source fitted to a legacy FIB platform.
We report herein the first-ever successful Cs-based circuit edits which were performed on 10nm Intel processors using the LoTIS tool. In addition, we present test results from a suite of tests characterizeing Cs suitability for nanomachining applications and Circuit Edit in particular. Our tests included: sputter and etch rates of common semiconductor materials, minimum micro-trench sizes, image resolution, beam profile characterization, amorphization ranges and contamination levels in common semi-conductor substrates, lack of invasiveness of Cs on 14nm Intel transistors, SE yield from several crystalline substrates, and electrical resistivities of FIB deposited dielectric and metal.

In summary, we comment on the suitability of Cs for Circuit Edit and additional nanomachining applications.

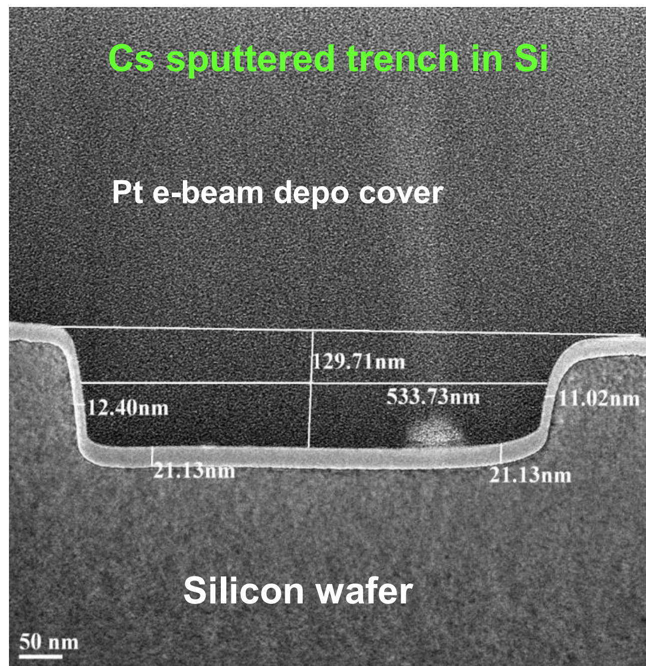

Fig 1. A bright field TEM cross-section of a 10 keV Cs sputtered trench in crystalline silicon. The light gray band seen on top of the silicon substrate is the amorphized silicon layer.

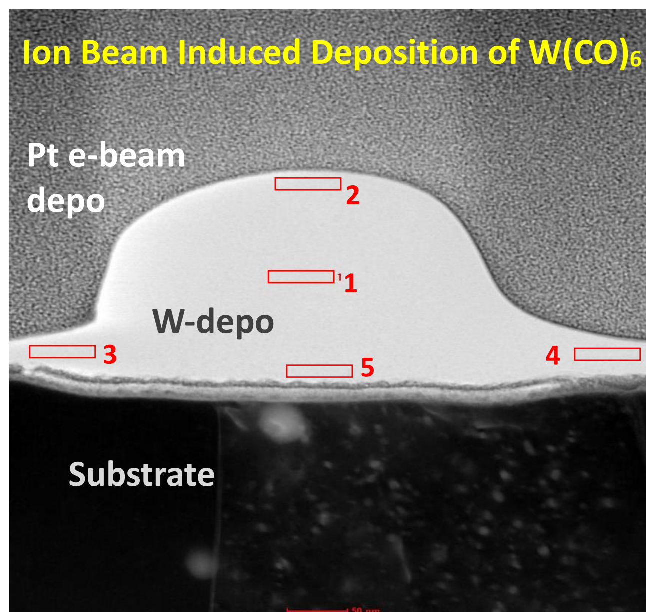

Fig 2. STEM cross-section image of a 10 keV Cs ion beam induced deposition of $W(CO)_6$ using a non-optimized FIB process. Elemental composition was analyzed by TEM EDS, and showed 75 at% carbon content.