Parametric Study of 2D Pulsed Laser Deposited (PLD) WSe_2 Transistors for enhancing an Infrared (IR) Detector

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Since the discovery of IR detectors two centuries ago, the technology has been harnessed in medical imaging, military equipment, environmental sensing amongst others [1]. The growing number of applications in highly sensitive thermal detectors in the mid-infrared range, requires ways of improving the responsivity and lowering the noise level of the devices [2]. An uncooled graphene based mid-infrared pyroelectric bolometer has been developed using $LiNbO_3$ crystal. The design sandwiched the graphene channel between the $LiNbO_3$ and a floating metallic gate which had been connected to the $LiNbO_3$. The pyroelectric charges from the $LiNbO_3$ crystal had been transduced onto the graphene thus modulating the graphene's resistivity hence a temperature coefficient of resistance several times greater than metallic and semiconducting bolometers had been realized [3]. Two Dimensional (2D) Transition Metal Dicalcogenide (TMD) materials, particularly WSe_2 has shown promise in electronic and optoelectronics devices, where the band gap increases and transforms to a direct band gap with decreasing number of layers [4]. Few-layer WSe_2 has been produced via the scotch tape method and via pulse laser deposition (PLD), on which Field Effect Transistors (FETs) have been fabricated and characterized [5] [6]. By integrating a WSe_2 FET with a pyroelectric detector, the performance of the IR device could be improved.

In this work, a back-gated PLD WSe_2 FET has been fabricated with different dimensions: Length (5 – 1000 μm) and Width (5 – 1000 μm). The schematic diagram for the fabrication process is shown in Fig 1(a). After the monolayer WSe_2 has been deposited via PLD on a 1*1cm SiO_2/Si substrate, the uniformity and structural characteristics of the WSe_2 films has been analyzed using Raman spectroscopy, see Fig 1(b). The channel patterns have been formed via optical lithography using a mask-less aligner, the design of the devices is shown in Fig 1(c). WSe_2 has been etched using controlled XeF_2 vapor and the metal contacts (Ti/Al stack) of the FETs deposited via E-beam evaporation and lifted-off.

To target an optimized device dimension for an integrated system, the electrical properties of the WSe_2 FET such as transfer curves and output characteristics will be investigated. The effects of hysteresis and charge trapping will be studied.

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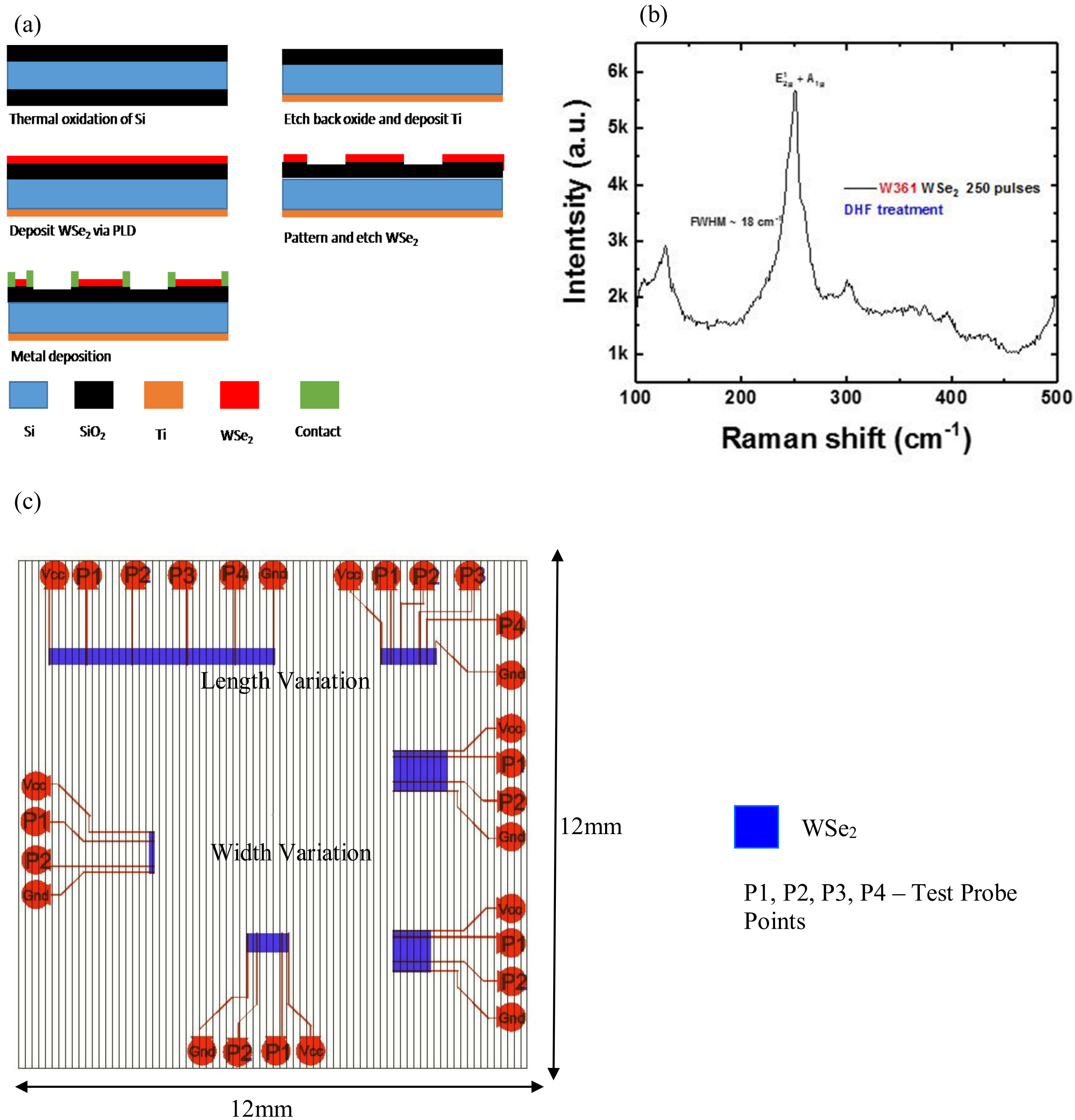

FIG. 1: (a) Schematic of WSe_2 FET fabrication. (b) Raman spectroscopy of PLD WSe_2; the peak at 250cm^{-1} denotes the presence of WSe_2 film. (c) Optical lithography pattern of FETs; the channel length is varied (5 – 1000 μm) as shown from the pattern at the top while the width is varied (5 – 1000 μm) as shown at the bottom.