Scalable fabrication of triangular nanopore membranes on sapphire substrate for low-noise DNA detection

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DNA sequencing has proven an invaluable tool in biology, early disease diagnosis, forensics, etc. Electronic DNA sequencing devices, such as solid-state nanopores, have the potential to achieve high-speed and low-cost electrical detection, but currently suffer from a high noise associated with its large device capacitance that originates from the interface between electrolyte and the silicon (Si) chip cavity. As a result, the Si-based nanopore platforms inherently suffer from a large current noise and limited bandwidth. To minimize the device capacitance, conventional approaches either manually introduce an additional insulating layer [1, 2] at the nanopore vicinity or using insulating glass substrate [3] to eliminate the capacitance. However, these approaches are rather complex, not scalable, and not feasible for precise control of the nanopore membrane dimensions.

In this study, we present and demonstrate a novel manufacturable approach to create thin membranes with well-controlled dimension and shape on a crystal sapphire wafer, which completely eliminates the large capacitance from the membrane cavity. Uniquely, we make use of the six-fold symmetry of the sapphire lattice to design triangular membranes (Figure 1), and demonstrate wafer-scale patterning of such membranes by anisotropic sapphire wet etching. Here, a thin layer of SiO_2 was used as a mask layer at both sides for etching through the sapphire (Figure 1a-c), where the SiO_2 window size L_1 determined the final membrane size L_2 (Figure 2d). We demonstrated that it was feasible to control L_2 down to 5μm, corresponding to a <2 pF capacitance even for atomically thin membranes in high signal-noise-ratio (SNR) [4] DNA detection. Such a capacitance would be about 2-3 orders of magnitude better than that on Si. We further created thin (32 nm) SiN_x membrane by sacrificing the SiO_2 membrane layer, and drilled a nanopore in SiN_x by transmission electron microscopy (TEM) for noise characterization and DNA sensing (Figure 3). We found that a relatively large SiN_x membrane on sapphire (8366 μm^2, or a membrane capacitance of 16.2 pF) still showed a >2.2 times smaller root-mean-square (RMS) ionic noise current compared to a much smaller membrane on a Si-substrate chip (31 μm^2 area and 0.1pF membrane capacitance). Given $I \propto C$ at high frequency, the result indicates further reducing the sapphire chip membrane capacitance to 1-2 pF (or the measurement system capacitance) would further lower its noise current, estimated ~20 times better than a Si chip.

The wafer-scale manufacturing uniformity, small device capacitance, and optical transparency make our sapphire membrane an advantageous and versatile platform. Additionally, the sapphire chips are compatible with a variety of promising electronic sensor designs, making it a versatile platform in future development of compact, inexpensive, and high-accuracy electronic detectors of a wide-range of biomolecules, from DNA/RNA to proteins, microvesicles, *etc.*

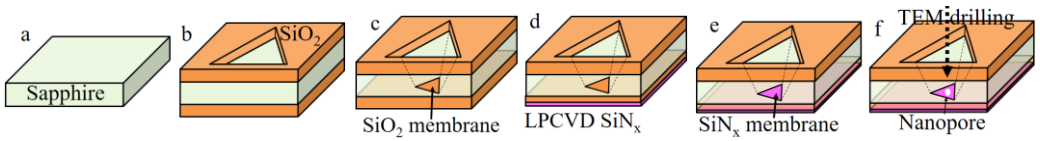

Figure 1: **Schematic showing the key steps for membrane formation and nanopore fabrication on sapphire**. (a) A 250μm sapphire wafer was used for fabrication. (b) A layer of PECVD SiO_2 was deposited on both sides, followed by lithography and RIE etching to define the sapphire etching mask. (c) The sapphire was etched through in hot sulfuric acid and phosphoric acid, forming suspended SiO_2 membrane. (d) A layer of LPCVD SiN_x was deposited on SiO_2 membrane, and the SiN_x in the cavity was etched by RIE to expose the SiO_2 membrane. (e) Thin SiN_x membrane was formed by first selectively removing the SiO_2 membrane in the cavity by hydrofluoric acid and then selective SiN_x thinning by hot phosphoric acid. (f) TEM was used to drill a nanopore in the SiN_x membrane.

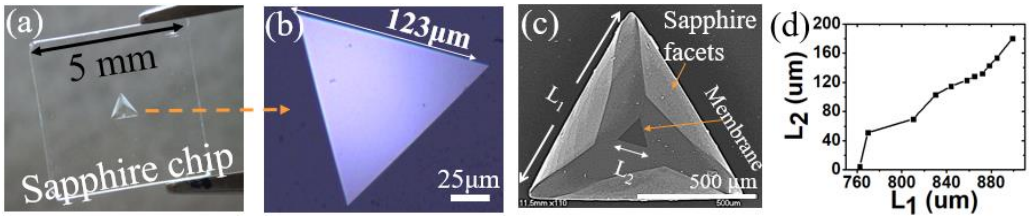

Figure 2: **Fabricated Sapphire chip.** (a) Photograph of a 5 mm sapphire chip. (b) Optical image of the suspended SiO_2 membrane (~3 μm thick) after sapphire etching. (c) SEM images showing the sapphire facets and the SiO_2 membrane. (d) Relation between the final membrane size L_2 and the window size L_1.

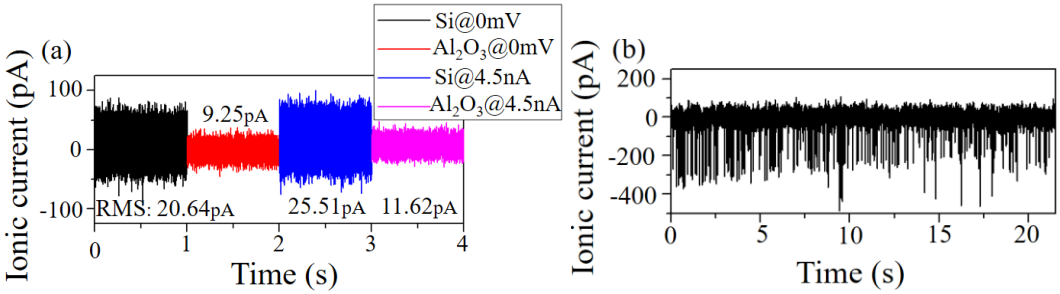

Figure 3: **Electronic characterization of sapphire nanopore chip.** (a) Baseline ionic current noise traces comparison between the SiN_x/Si chip and the SiN_x/sapphire chip. The sampling frequency is 250 kHz and the filter frequency is 10 kHz. (b) 1kbp ds-DNA signals collected from the SiN_x/sapphire chip, with the baseline adjusted. The low pass filter frequency and the sampling frequency is 10 kHz and 250 kHz respectively and the voltage is 200mV.

References:

[1] J. K. Rosenstein *et al.*, Nature methods **9**, 487 (2012).
[2] S. Shekar *et al.*, Nano letters **16**, 4483 (2016).
[3] A. Balan *et al.*, Scientific reports **5**, 17775 (2015).
[4] M. Wanunu *et al.*, Nature nanotechnology **5**, 807 (2010).

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