Low-contrast electron beam lithography process for fabrication of sloped sidewall HSQ spacers

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Contact vertical interconnect access (via) fabrication is one of the fundamental steps of the back end of the line (BEOL) portion of IC fabrication, allowing device interconnection and facilitating vertical integration. However, standard CMOS via processes may not be easily integrated in the fabrication flow of novel emerging devices. In such situations, to allow layers vertical stacking or multilevel devices fabrication, a different approach in electrical isolation and connection is necessary.

In this work, we propose the fabrication of sloped sidewall dielectric spacers to provide device separations while preserving metal traces continuity (Fig. 1). 3D surface topography is generally obtained by gray-scale electron beam lithography (GEBL). However, it requires fine control of the exposure dose [1]. Methods based on resist reflow require long baking processes with potential degrading impacts on devices [2]. Here, through a specifically designed low-contrast EBL process, we exploit the normally-unwanted side exposure from backscattered electrons and resist non-idealities [3] to create sloped sidewall profiles.

HSQ (FOX-16) is spun to a thickness of ~ 500 nm and thermally cured at 250 °C for 2 minutes. It is then exposed using 125 kV electron beam lithography, providing a dose of 800 $\mu C/cm^2$ with 20 nA current, and then developed in diluted TMAH (2.6%) for 90 s. To demonstrate the effect more clearly, we have patterned $100\ \mu m \times 100\ \mu m$ dummy squares on 300 nm thermal oxide on Si substrate (Fig.2). The exposure dose intensity has been simulated by using the "e-beam" module in BEAMER, importing the beam PSF simulated using TRACER (both softwares from GenISys). The obtained feature profile has been measured with a profilometer and compared to the effective exposure dose in Fig.3a. A partial resist contrast curve is extracted by comparing the obtained sidewall profile with the effective dose (Fig.3b). The obtained sloped HSQ pattern allows the electrical continuity of metal traces going above (Fig.1b) while isolating underneath devices. Applications where metal continuity is essential for signal propagation and integrity (ground continuity in microwave devices) may benefit from this fabrication process.

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[2] Kirchner, R. et al. *Microelectronic Engineering* 153 (2016): 71-76.
[3] Olynick, Deirdre L., et al. *Journal of Vacuum Science & Technology B* 24.6 (2006): 3048-3054.

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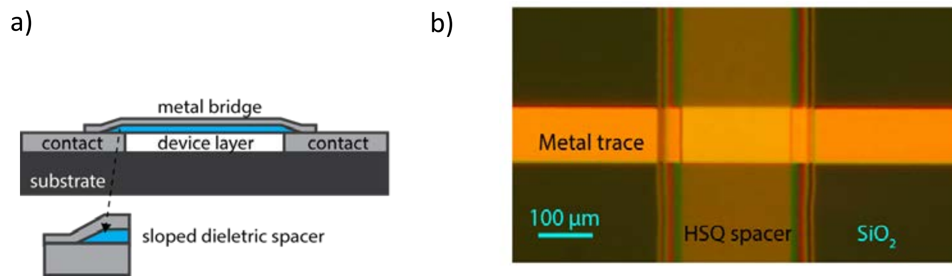

Fig.1: a) Conceptual application of sloped sidewall HSQ spacer: the physical presence of the spacer allows device layer isolation, the sloped sidewall facilitate metal trace continuity; b) optical micrograph of a metal trace over the dielectric spacers.

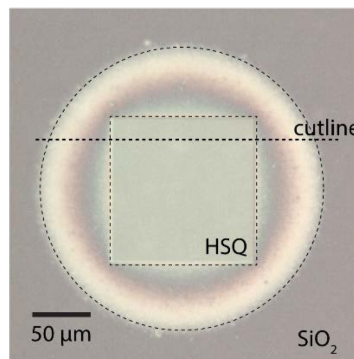

Fig.2: Optical micrograph of a 100 µm × 100 µm HSQ square patterned with the low contrast process. The square pattern is surrounded by a circular shape due to side exposure from backscattered electrons creating the slopes profile.

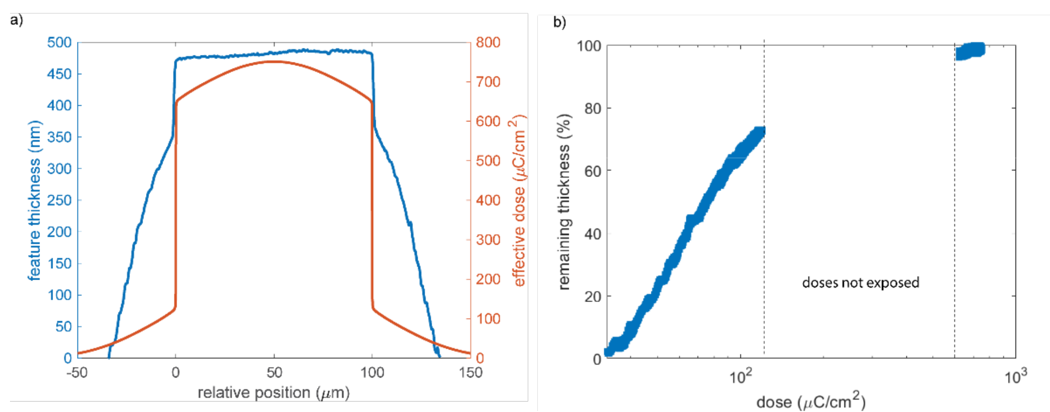

Fig.3: a) Comparison between the simulated dose profile (using BEAMER and TRACER from GenISys) and the measured feature: the side exposure results in the sloped profile; b) a partial contrast curve is extracted by feature-dose direct comparison.