Nanoscale Lift-Off Process Using Field-Emission Scanning Probe Lithography

Martin Hofmann^{1, *}, Stephan Mecholdt¹, Mathias Holz², Ahmad Ahmad^{1,2}, Tzvetan Ivanov¹, Eberhard Manske³, and Ivo W. Rangelow¹

¹Dept. of Micro- and Nanoelectronic Systems, TU Ilmenau, Gustav-Kirchhoff-Str. 1, 98693 Ilmenau, Germany

²Nanoanalytik GmbH, Ehrenbergstraße 1, 98693 Ilmenau, Germany ³Institute of Process Measurement and Sensor Technology, TU Ilmenau, Gustav-Kirchhoff-Str. 1, 98693 Ilmenau, Germany

hofmann.martin@tu-ilmenau.de

The nano-electronics manufacturing is based on the ongoing development of the lithography and encompasses also some "unconventional" methods. In this context, we use field emission scanning probe lithography (FE-SPL) to generate nano-scaled features in ultra-thin (10 nm) resist layers. Therefor we built a FE-SPL-and-AFM platform combine FE-SPL and AFM using the same (active) cantilever. This lithographic method has been explained in a previous publication [1]. The utilization of self-sensing and self-actuated scanning probes enables us to use two independent feedback loops in our setup: a feedback loop for the AFM and a second as a current-control feedback for FE-SPL (Fig. 1) [2].

For the generation of future novel quantum devices such as single electron transistors or plasmonic resonators, patterning of features in the sub-10 nm regime as well as a defined metallization is required. Previously the capability of a SET working at room-temperature written by FE-SPL was presented [3]. In this work we further push our FE-SPL-and-AFM platform towards an all-in-one patterning and analysis tool by establishing a defined precise nanofabrication of metal features for the generation of quantum and single electron devices.

Since FE-SPL uses very thin (~ 10nm) resist, an efficient pattern transfer in metals like Cr, Al or Au is not possible. Furthermore, a disturbance of underlying sensitive materials is possible. Therefore, we take advantage of the well-known lift-off process, already realized for different state-of-the-art lithography techniques.

In lift-off processes presented here (fig. 2) two sacrificial layers (50 nm polymethylglutarimide (PMGI) and 10 nm calixarene), have been deposited and patterned by FE-SPL on a silicon substrate. Subsequently, the sample was treated with TEAH in order to ensure an undercut. Afterwards, a layer of 10 nm thick Cr has been deposited on top and the sacrificial resist films have finally been removed, leaving behind only the chromium film deposited directly on the substrate.

In this work we will present the utilization of diamond tips [4] for FE-SPL purposes in order to generate chromium metal features by lift-off for the generation of future quantum devices. Those features can be seen in fig. 3. Here, the applied bias voltage was 75V, whereas the line dose was 500 nC/cm.

- [1] Rangelow, I.W. et. al., Proc. SPIE, 7637 (2010).
- [2] Kaestner, M. et. al., Proc. SPIE, 8323 (2012).
- [3] Rangelow, I.W. et. al., JVST B 34, 06K202 (2016).
- [4] Hofmann, M. et. al., JVST B 36, 06JL02 (2018).



Fig. 1: Concept of closed-loop for imaging and patterning by an active cantilever.



Fig. 2: Basic principle of the conducted lift-off process.



Fig. 3: AFM image of chromium SET features after lift-off. Contour of the gap between two features was conducted at the position inclined by the white line in the AFM image.