

# Fabrication and Characterization of Multilayer Heater-Cryotrons

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High-speed, low-power, nanoscale superconducting switches are essential in realizing superconducting electronic circuits. In recent years, there have been many attempts to develop electro-thermal superconducting switches based on the destruction of superconductivity in the channel by running a small current to the gate [1]. These superconducting 3-terminal devices, also called nano-cryotrons (nTrons), have a planar structure and are monolithically fabricated on a thin-layer superconducting film. The nTrons are known as fast superconducting switches and have many applications in classical and quantum computing, readout of detector arrays, memories, multiplexers at cryo-temperature testing. Although these devices have been very successful in demonstrating fast nanoscale superconducting switches, they face significant challenges related to sneak current and low fan-out.

To overcome the sneak current issue in the nTron, planar heater-cryotron (P-hTron) devices were developed [2]. In a P-hTron, the heater is a superconducting nanowire placed next to the channel. Since the heater is electrically isolated from the channel, the sneak current is not an issue anymore. However, P-hTrons face issues like latency and demanding fabrication processes to make vias to allow crossovers.

To address these issues, we investigated multilayer-hTrons (M-hTron) where the heater is placed on top of the superconducting channel and is galvanically isolated from the channel by placing a thin layer of an oxide film between the heater and the channel. The heater is made of a normal metal that allows suppression of the channel's critical current in a controllable manner.

The fabrication of M-hTrons requires a multistep electron-beam lithography (EBL) process that introduces several challenges. In the first step, gold alignment marks are patterned on top of a 20-nm-thick NbN film using a lift-off process. The superconducting channel is realized on the NbN film by using EBL and reactive ion etching (RIE). The entire chip is then covered by a 10 nm-thick sputtered Si layer. The heater, made of a bilayer of SiO<sub>2</sub>/Ti/Pt (35/25/10 nm), is defined on the top of the superconducting nanowire channels by using a lift-off process. The SiO<sub>2</sub> layer isolates the heater electrically from the channel, thus preventing sneak currents. Fig. 1 shows the colored scanning electron microscope (SEM) image of a fabricated M-hTron device.

We performed various characterizations on M-hTron devices. Studies of the switching current, as a function of the heater's current, showed that the channel's switching current smoothly reduces as the heater's current increases (see Fig. 2). We also fabricated several M-hTron devices with varying channel widths ranging from 100 nm to ~10 μm. We learned that the amount of current required to suppress the switching current of each device to its retrapping current is only 10% higher for 10 μm-wide wires when compared to a 100-nm-wide channel.

In summary, we successfully fabricated and tested multi-layer three-dimensional superconducting switches. These hTrons overcome the undesired sneak currents in nTrons and they offer high fan-out, which makes them very suitable for developing compact superconducting circuits.

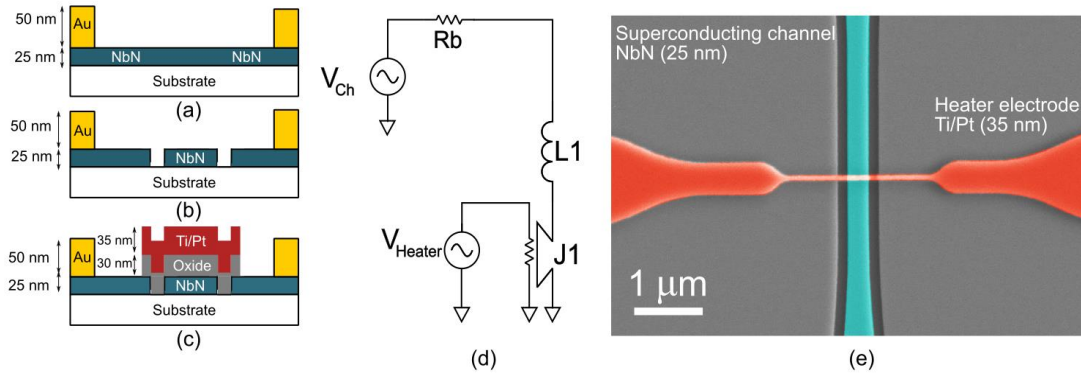


Figure 1: Cross section view of the fabrication process. (a) Au marks are defined on 25-nm-thick NbN film using the lift-off process. (b) The superconducting channel is then realized on the NbN film using the RIE process with CF<sub>4</sub> gas. (c) A heater made of a bi-layer of Pt/Ti is defined on the top of the superconducting channel. A 25-nm-thick layer of the SiO<sub>2</sub> layer is employed as a dielectric layer, isolating the heater and the channel. (d) Schematic design of a hTron device. The channel is made of superconducting NbN film. The heater is a normal metal heater which is thermally coupled to the superconducting channel. (e) Colored scanning electron microscope image of a fabricated M-hTron device. The heater (red) is galvanically isolated from the superconducting channel (blue) by a thin layer of SiO<sub>2</sub>.

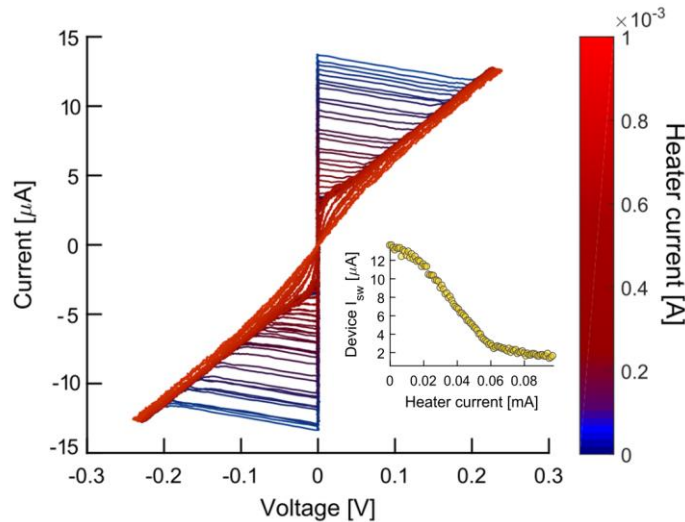


Figure 2: Current-voltage characteristics of the channel as a function of the heater's current. Upon increasing current to the gate the switching current reduces.

#### References:

- [1] McCaughan, Adam N., and Karl K. Berggren. "A superconducting-nanowire three-terminal electrothermal device." *Nano letters* 14.10 (2014): 5748-5753.
- [2] Zhao, Qing-Yuan, et al. "A compact superconducting nanowire memory element operated by nanowire cryotrons." *Superconductor Science and Technology* 31.3 (2018): 035009.