(Invited) Progress, challenges and outlook of three-dimensional hybrid CMOS/ReRAM systems

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This work is focused on building 3D analog ReRAM crossbars, both standalone and monolithically integrated with CMOS, and using them for prototyping promising applications in neuromorphic computing (Figure 1). The thermal budget, yield and switching uniformity have to be considered during the fabrication of such multi-stack systems. Non-destructive characterization methods have been developed to help with device optimization (Figure 1a) [1]. Firstly, we reported a monolithic back-end-of-line integration of two Pt/Al_2O_3/TiO_{2-x}/TiN/Pt -based passive crossbars with shared middle electrode (Figure 1b) [2]. The devices in these crossbars demonstrated a repeatable and strong STDP response. Secondly, we demonstrated a hybrid CMOL architecture with two layers of ReRAM crossbars monolithically integrated on a pre-fabricated CMOS substrate (Figure 1c)[3]. The two crossbars can be fully operated by the underlying CMOS circuitry and exhibit analog switching behavior with controlled tunability. Dot-product operations were performed to demonstrate the applicability of 3D CMOL circuits as a multiply-add engine.

Despite recent progress in the field, there are still major challenges hindering large scale adoption of these systems. Device variability is a costly drawback for neuromorphic computation, despite its resilience to hardware defects. If device-to-device and cycle-to-cycle variability affects a ReRAM crossbar, programming to a desired state becomes a personalized endeavor. This approach is not practical for tuning billions of ReRAM devices, as it consumes time, energy and chip real-estate for supporting circuitry. Exhaustive material and device engineering are needed, but in the meantime algorithmic solutions, such as batch training, can help alleviate these challenges (Figure 1d). [4]

A potential roadmap towards realizing competitive memristive-based systems will be presented (Figure 2) [5]. Issues requiring short vs. long term attention will be discussed. Ultimately though, the balance between system-level performance vs. manufacturing cost will be the drive behind widespread adoption.

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[1] Hoskins, B. D. et al. Nature Communications, 8(1), 1972, 2017.
[2] Adam, G. C. et al. IEEE Transactions on Electron Devices, 64(1), 312-318, 2017.
[3] Chakrabarti, B. et al. Scientific Reports, 7, 42429, 2017.
[4] Hoskins, B.D. et al. ArXiv, https://arxiv.org/ftp/arxiv/papers/1903/1903.01635.pdf, 2019.
[5] Adam, G. C. et al. Nature Communications, 9(1), 5267, 2018.

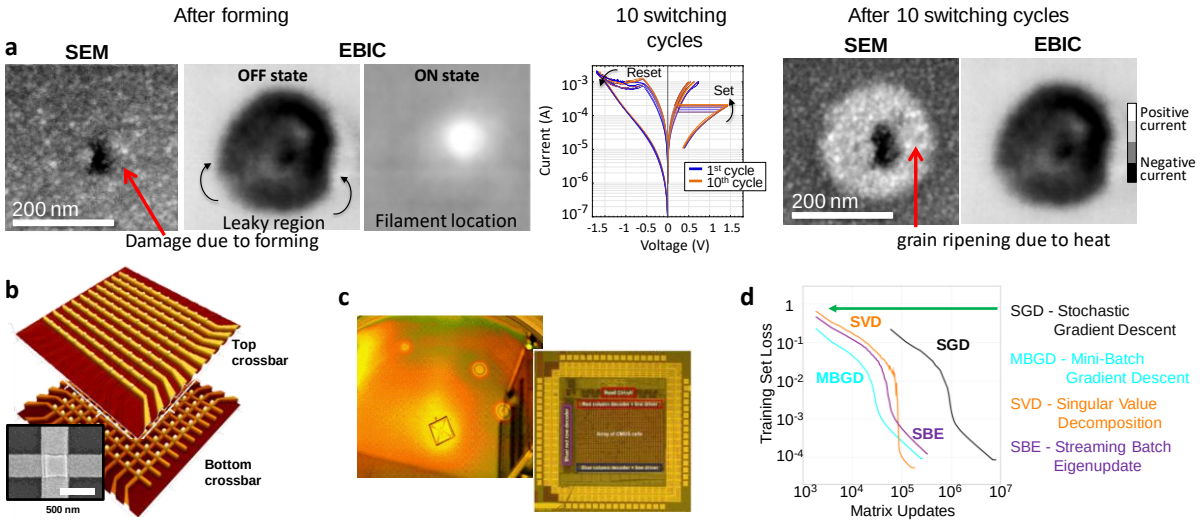

Figure 1: From ReRAM device engineering to hybrid CMOS/ReRAM systems. (a) Non-destructive EBIC characterization showing leaky region near the filament leading to damaging grain ripening after 10 switching cycles. Material engineering to solve this problem leads to improved device reproducibility. (b) Three-dimensionally stacked ReRAM crossbars (standalone) and (c) integrated with CMOS circuitry enabled thanks to the improved device reproducibility; (d) Batch training vs. stochastic training improved results in terms of crossbar updates overhead.

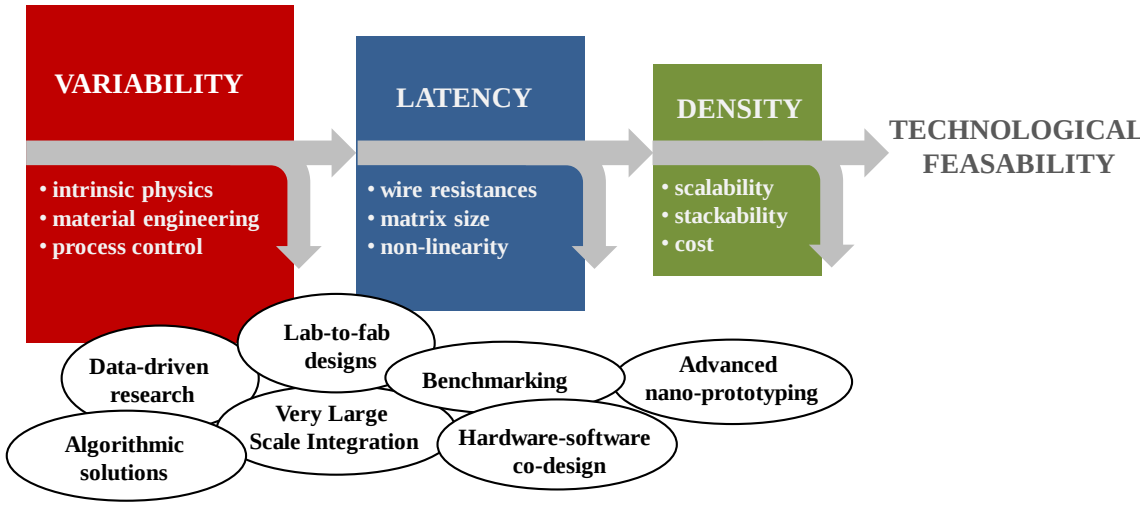

Figure 2: Roadmap for challenges in fabrication of hybrid CMOS/ReRAM-based systems.