Progress Toward 2D Nano Bipolar Junction Transistors

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Abstract: Zyvex Labs is exploring two dimensional nanoscale bipolar junction transistors that are created with delta-doped donor and acceptor patterns on a single (100) plane, buried in Si. These patterns are created by Hydrogen Depassivation Lithography (HDL)[1]. The process will involve sequential stages of HDL patterning and dosing with appropriate precursor gases[1,2] for t separate donor and acceptor patterns, followed by low temperature Si epitaxy to bury the device components[3]. These techniques have been used with donors to make atomic-scale quantum and analog devices[4].

This fabrication technique should be able to create very high performance small signal analog bipolar junction transistors. The reasons are: 1)atomic precision patterning of nm-scale[5] emitters, bases, and collectors will provide very high gain-bandwith products; 2) extremely good control of the number of dopants in each element due to the self-limiting deposition of dopants on the surface[6] will provide excellent control of device properties and unprecedented matching 3) the very high doping levels available with delta-doping[6] used both for the devices and wiring between devices, have extremely low-noise conduction[7] and remain conductive at cryogenic temperatures[8]. 4) the devices' extremely small volume and distance from any material interfaces will make them very rad-hard. There has been modelling of scaled bipolar devices that supports very high performance[9].

The very small base dimensions and very high doing levels possible will undoubtably lead to some interesting quantum effects in the form of intraband tunneling (Ezaki diode junction) and confined energy levels in the base. Modelling is planned but only experiments will determine the nature and impact of these quantum effects.

In this presentation we will discuss early progress in attempts to develop delta doped PN junctions and the use of implanted regions to make excellent ohmic contact to the delta doped regions, reduce the amount of HDL lithography required, and to realize a novel 2D-3D-2D NPN transistor. In our process flow (Figure 1) the implants will come first and are designed to achieve 1x10E19 dopants/cm^3 for both P and B implants from the surface down to ~100nm. Instead of having to expose large areas with HDL we can use the implanted region to create an easy to align to contact area. An HDL patterned device lead will only have to pass over a small section of the implanted region to make a good ohmic contact and deposited metal ohmic contact to the implanted regions will be trivial. The closer we can place these implanted regions to the devices, the less time we need to spend doing HDL writing the leads. However, there will be lateral diffusion during the high temperature (1200°C) surface preparation before HDL. Process simulation of the implant and diffusion processes are shown in Figure 3. We have designed some test structures to experimentally measure the diffision at cryogenic temperatures.

We expect to be able to fabricate and measure 2D PN diodes using the process shown in Figure 1 where we expect to see the transport of an Ezaki diode. We also hope to fabricate and measure a 2D NPN bipolar transistor by using an implanted Boron region as a base as shown in Figure 2. Initial measurements will be done at cryogenic temperatures which will freeze out parasitic conduction paths.

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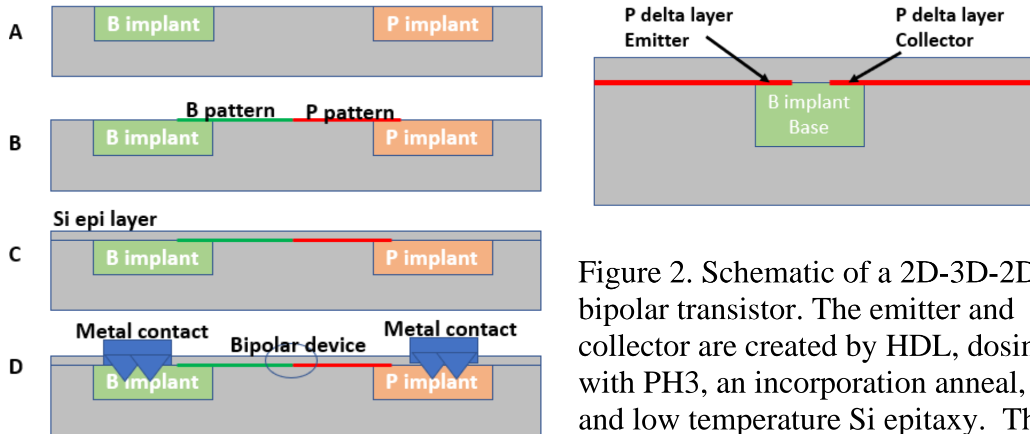

Figure 1. A) Acceptor (Boron) and donor (Phosphorous) implants are activated by high temp sample prep for HDL. B) HDL, dosing, and anneal creates patterned delta layers. C) low temp Si epitaxy D) deposition and anneal of metal contacts.

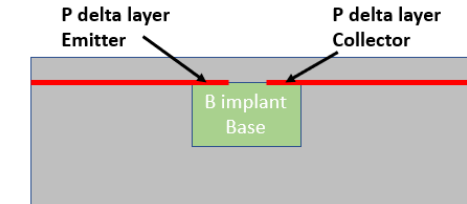

Figure 2. Schematic of a 2D-3D-2D bipolar transistor. The emitter and collector are created by HDL, dosing with PH3, an incorporation anneal, and low temperature Si epitaxy. The base is formed by a boron implant region. The contacts to emitter, base, and collector are not shown but are similar to Figure 1.

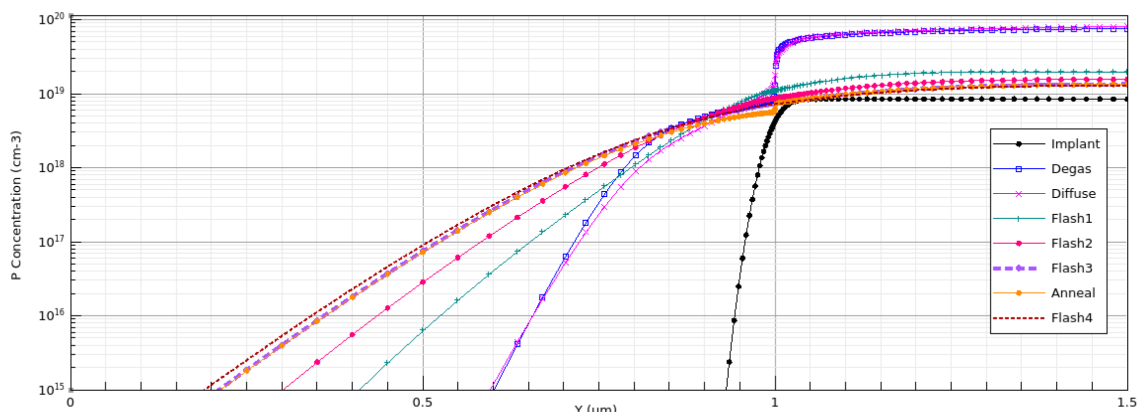

Figure 3. Simulation of implant and diffusion after a number of annealing steps required for HDL sample preparation of P into Si. The data for B shows less lateral diffusion. The data suggests that spacings greater than 1um should avoid conduction between implants at cryogenic temperatures.