Comparison of alignment markers and method for electron-beam lithography on CMOS dies

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Back-end-of-line (BEOL) integration of microelectronic devices above CMOS integrated circuits has attracted a lot of attention in the last decade either to increase device density or add functionality. Demonstrations have already been shown for in-memory computing applications[1], quantum computing[2] and integrated nano-photonics[3]. For that purpose, electron-beam lithography (EBL) is a powerful platform for R&D and prototyping that provides design and layout flexibility together with high-resolution capability down to nanoscale for emerging technologies development.

BEOL materials, more specifically thick dielectric materials and design rules are fixed for each CMOS technology node and represent challenges for both the EBL of nanostructures and the alignment with the last metal levels patterns. Cu damascene technology forces the use of dummy structures that do lead to design rules specific to each CMOS node. Those rules impede maximal and minimal dimensions as well as spacing that do not allow the drawing of large clear space around the marks to perform linescan as shown in Fig.1. Image correlation is a strategy that can be exploited for the EBL alignment. In this paper, we will discuss the challenges in terms of EBL and alignment on top of a 130 nm integrated circuit and present an alignment procedure using image correlation. The overlay of two lithography levels will be used as a vehicle for our tests to quantify the accuracy of the alignment process as shown in Fig.2. Different markers are proposed and their performances in terms of processing and overlay accuracy will be detailed.

The alignment tests were done with a 100 keV Raith EBPG5200 electron beam lithography system using a 1 mm write field. The lithography was carried out using a single layer of resist with the sample being unloaded and reloaded in the system between lithography levels. The samples were developed, test structures patterned were imaged using SEM and the overlay accuracy measured by GenISys ProSEM software. The analysis shows an alignment precision better than 5 nm in both X and Y directions.

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[1] Cai, F. *et al*. *Nat Electron* **2,** 290–299 (2019).
[2] Kim, D. *et al*. *Nat Electron* **2,** 284–289 (2019.
[3] Y. A. Vlasov, , *IEEE Commun. Mag.*, vol. 50, nº 2, p. s67-s72, (2012).

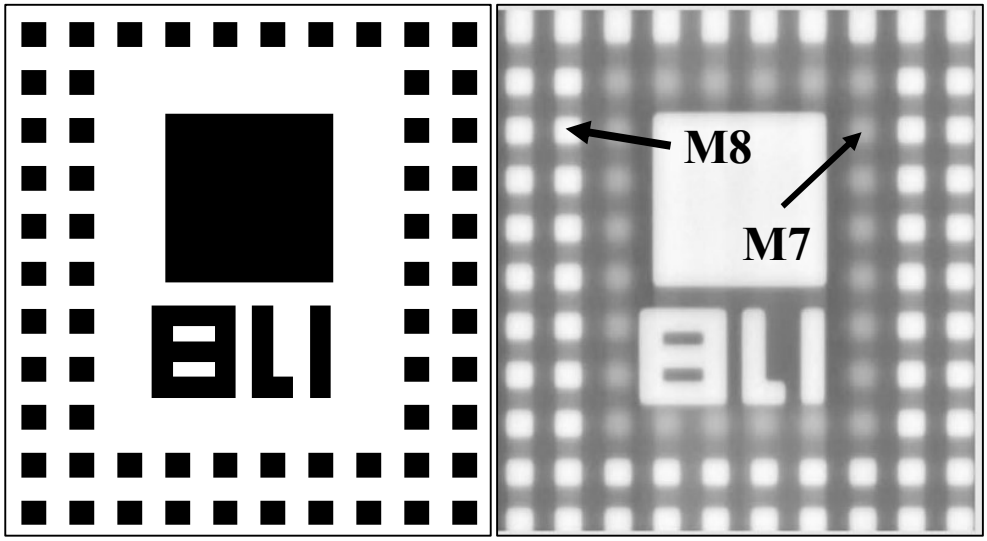

Figure 1: Alignment Mark on CMOS. On the left: Layout of the last metal level (M8) with squared dummies. On the right: Backscattered electrons image captured by the EBPG at 100keV. Highlighting: (i) that the design rule does not allow large clear space around the markers to perform linescans; (ii) M7 Cu structures underneath M8 are also detected disturbing the alignment.

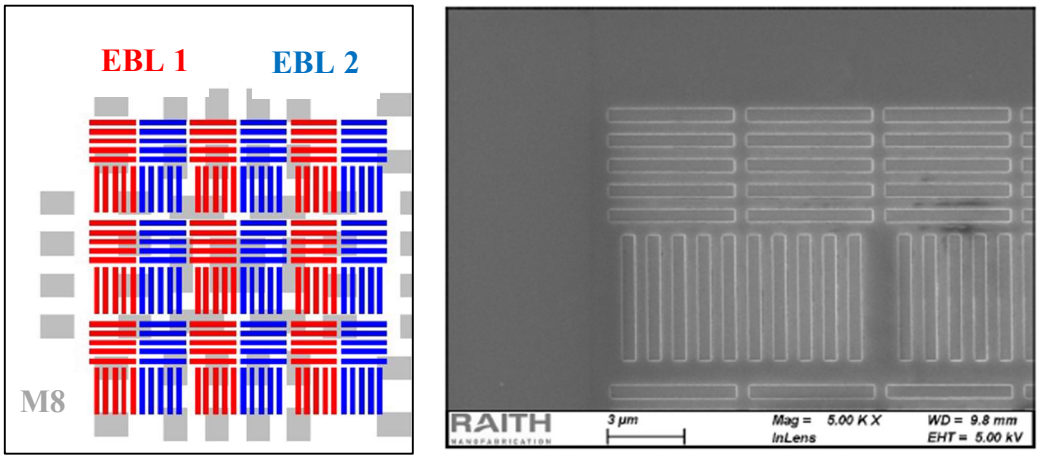

Figure 2: Overlay Test. On the left: layout of the overlay test performed in two steps in a single layer resist. The first lithography (EBL 1 / red) is aligned on M8; the sample is unloaded and reloaded into the system; the second lithography (EBL 2 / blue) is carried with a similar procedure than EBL 1. The sample is developed and imaged by SEM as shown on the right. The overlay accuracy measured by GenISys ProSEM software shows an alignment precision better than 5 nm in both X and Y directions.