Chip-scale fabrication of FETs by a combination of thermal scanning probe lithography and direct laser sublimation

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Thermal scanning probe lithography (t-SPL) uses a heatable ultra-sharp tip for patterning thermal resists and simultaneous inspection of the nanostructures being patterned [1]. The technology has proven its value as an enabler of new kinds of ultra-high resolution nanodevices [2] as well as for improving the performance of existing device concepts [3]. Therefore, t-SPL offers the first true alternative or a complementary extension to other mask-less nanolithography methods such as electron beam lithography (EBL).

The range of applications for t-SPL is very broad [1] spanning from ultra-high resolution 2D and 3D patterning to chemical and physical modification of matter at the nanoscale. Nanometer-precise markerless overlay and non-invasiveness to sensitive materials are among the key strengths of the technology. However, while patterning at below 10 nm resolution is achieved, significantly increasing the patterning speed at the expense of resolution is not feasible by using the heated tip alone. Towards this end, an integrated laser write head for direct laser sublimation (DLS) of the thermal resist has been introduced for significantly faster patterning of micrometer to millimeter-scale features [4]. Remarkably, the areas patterned by the tip and the laser are seamlessly stitched together and both processes work on the very same resist material enabling a true mix-and-match process with no developing or any other processing steps in between.

Here, we demonstrate how the combined tip and laser patterning has been used for the first time for chip-scale fabrication of complete field effect transistor (FET) devices with channel widths in the 15 – 50 nm range (Figure 1). For patterning the gates, an automated markerless overlay algorithm correlating the device geometry with measured sample topography is applied enabling a fully automated patterning process over the entire chip. This work paves the way for t-SPL's development into a fully automated, high-precision nanolithography tool with a significantly increased throughput.

[1] S. T. Howell et al., *Microsyst Nanoeng* **6**, 21 (2020).
[2] M. J. Skaug et al., *Science*. **359** (6383), 1505–1508 (2018).
[3] X. Zheng et al., *Nature Electronics* **2**, 17-25 (2019).
[4] C. D. Rawlings et al., *Nanotechnology* **29** (50) 505302 (2018).

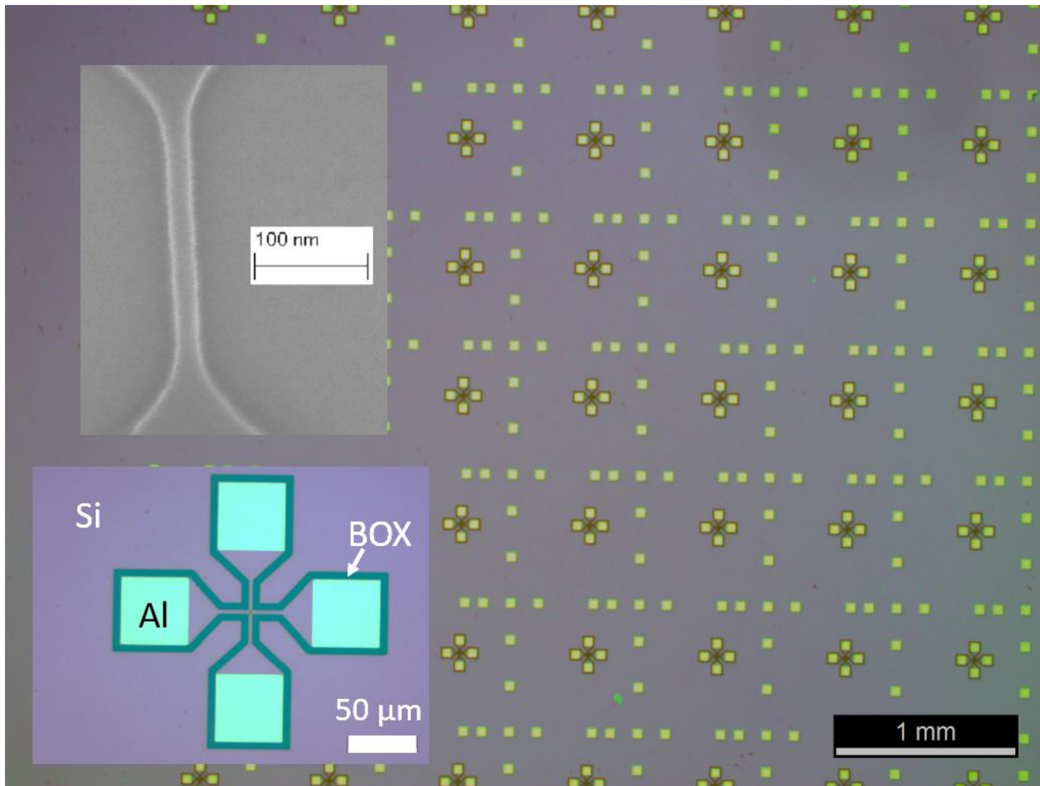

Figure 1: Optical micrograph of a FET array (here without top gates) on a silicon-on-insulator (SOI) chip. The contact pads and leads were patterned by laser and the fine features by t-SPL. Bottom left: An individual FET with Al contact pads. The exposed buried oxide is seen as a green rim around the electrodes. Top left: A scanning electron micrograph of a Si fin channel fabricated using thermal scanning probe lithography. The channel width is approximately 20 nm.