An Easy-to-fabricate Testing Chip for Electrical Characterization of Nano-particles

Ming Lu
Center for Functional Nanomaterials, Brookhaven National Laboratory, Upton, NY 11973
mlu@bnl.gov

With the development of synthesis methods for semiconductor and dielectric nanoparticles, there is a rise of needs to characterize the electrical properties of nanoparticles. While method has been developed for nanowires, by mapping the nanowires on the substrates and customizing electrodes in a case-by-case fashion, and may still work when applied to nanoparticles, it is even less efficient compared to already low efficiency when applied to nanowires. Delicate tools such as nanoprobe station are very expensive and need extensive expertise to operate properly. Here we introduce a method based on a low-cost and easy-to-fabricate testing chip, which only need several tens minutes to turn nanoparticles to ready-for-measurement samples.

The testing chip is illustrated in Figure 1, which is an array of metallic square pads sitting on the silicon dioxide layer of silicon substrate. The gaps between square pads are designed according to the size of nanoparticles, typically around one micron, which should be large than the largest particles to be tested. The silicon dioxide layer thickness should be sufficient to ensure insulation between adjacent metallic pads but should not be too thick if an external electrical field is expected to applied during the test. The material of metallic pads can be platinum or tungsten, depending the work function of the nanoparticle. Such kind of testing chip can be easily pre-fabricated using photolithography and lift-off process.

During test sample preparation stage, the solution-based nanoparticles are first dispensed to the surface of the testing chip and dried. The chip is then transferred into a Focused Ion Beam (FIB) SEM tool with EBID (Electron Beam Induced Deposition) capability. In SEM mode, those nanoparticles sitting in the gaps can be quickly identified and the metals such as platinum and tungsten can be deposited using EBID technique to form local contact connecting with the adjacent metallic pads. After that, additional metal bars can be deposition to connect selected pads to form conduction paths. Due to the small gap, EBID process only take several tens seconds each. The total time to prepare a chip for electrical measurement only takes several tens minutes.

The method introduced here only require a FIB-SEM with EBID capability. The chip can be fabricated at low cost from traditional microfabrication lab or be out sourced. It will greatly reduce the burden of nanofabrication for those nanoparticle synthesis research groups.

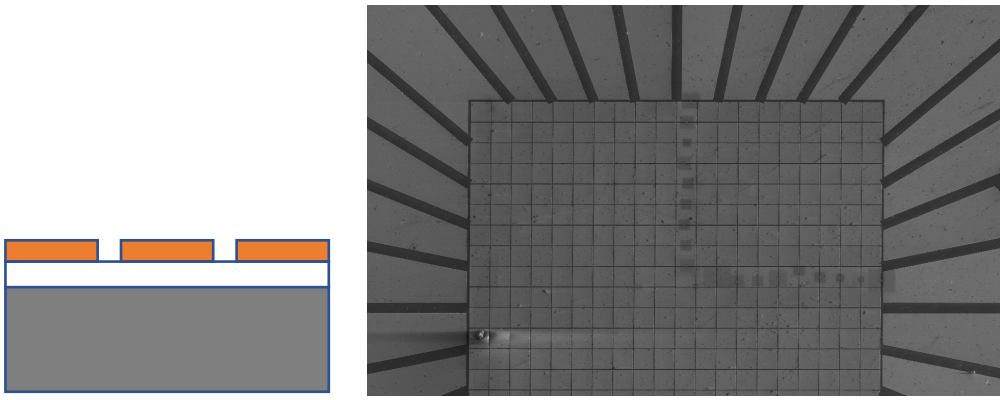

Figure 1: Design of a testing chip. Left: Cross-section illustration. The materials from top layer to bottom layer are metal, silicon dioxide and silicon. Right: Micrograph of part of a testing chip. The 20x20 metallic pad array is 200-micron-wide. Two contact paths can be identified along those pads bridged by dark spots.

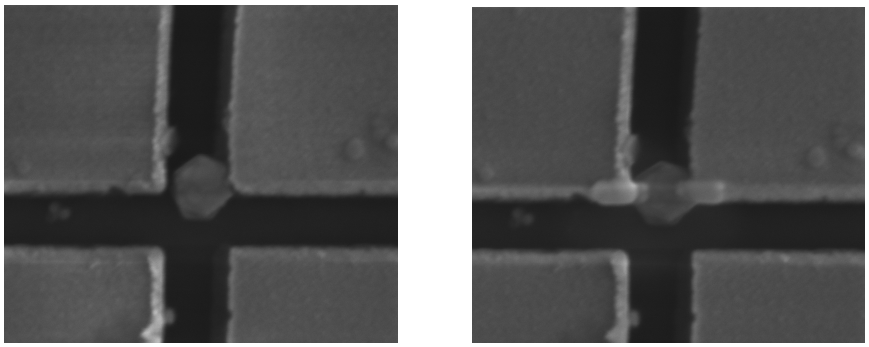

Figure 2: An example of metallic contacts deposition. Left: An ideal nanoparticle is identified in the gas between two pads. Right: Two platinum contact bars have been deposited to bridge the pads and the nanoparticle.

Research carried out at the Center for Functional Nanomaterials, Brookhaven National Laboratory, which is supported by the U.S. Department of Energy, Office of Basic Energy Sciences, under Contract No. DE-SC0012704.