Fabrication of Micro Chemical Vapor Deposition Chamber by Dry dry Deep Silicon and Metal-Assisted Etching Techniques

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To address the high speed and low latency requirements of the data transport in the memory devices, there is always a need for integration of ultra-high-density logic and memory[1]. The limitations of the highly explored silicon planar fabrication technology spurred the need to stack and interconnect the dies in 3D. Moreover, the design challenges in the 3D approach laid a new path towards building each layer in the stack by monolithic integral approach, which has higher yield. There is an acute need for developing disruptive ways of micro/nano fabrication to address the challenges of the three-dimensional monolithic fabrication[2].

Our goal is to demonstrate a process flow for the through silicon via (TSV) of ~500 nm and lower diameter opening (nozzle) on one end and 150 x 150 μm opening (reservoir) on the other end. This silicon die will be used as a micro chemical vapor deposition (CVD) chamber, which is a critical component in the nanoscale additive writing process. A detailed process optimizations for the nozzle and reservoir fabrication steps will be discussed.

Briefly, the miniaturized CVD chamber fabrication process starts with 2 μm device layer SOI wafer as shown in Fig. 1(a). The silicon is etched from the front and back side, using back side alignment and deep silicon etching to define the micro CVD chamber reservoir as shown in Fig. 1(b) and (c). The nozzles of ~500 nm and lower diameter are obtained by dry etching and metal assisted etching techniques[3] (MAE) respectively (Fig. 1(d)). The deep silicon TSV etch results showing 30 μm opening in 380 μm Si, aspect ratio 1:15, are presented in Fig. 2. We used the MAE approach to etch ~50 nm (1:40 aspect ratio) opening and dry etch for 3 μm, 2 μm and ~300 nm (Fig 3). Finally, the micro CVD reactor will be mounted on the additive manufacturing tool for the deposition.

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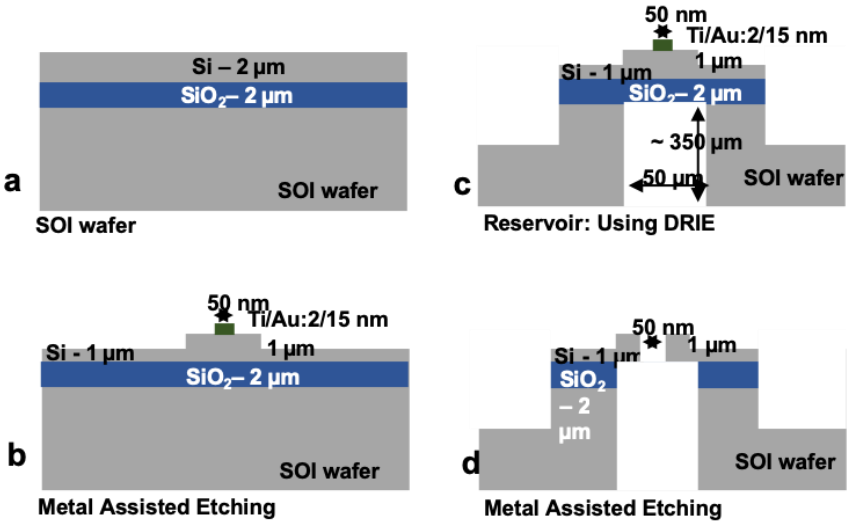

Figure 1. (a) Nanofabrication process flow of micro CVD reactor fabrication on a SOI wafer. (b) E-beam evaporation of Ti/Au: 2/15 nm and 1 µm silicon etch using reactive ion etching. (c) Deep reactive ion etching (DRIE) to form CVD precursor cavity. (d) 50 nm nozzle opening using metal assisted etching and oxide etch.

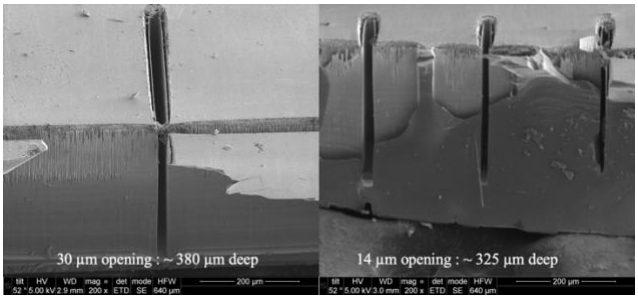

Figure 2: SEM image of 380 µm deep silicon dry etch for 30 µm opening (left) and ~325 µm deep etch for a 14 µm opening (right).

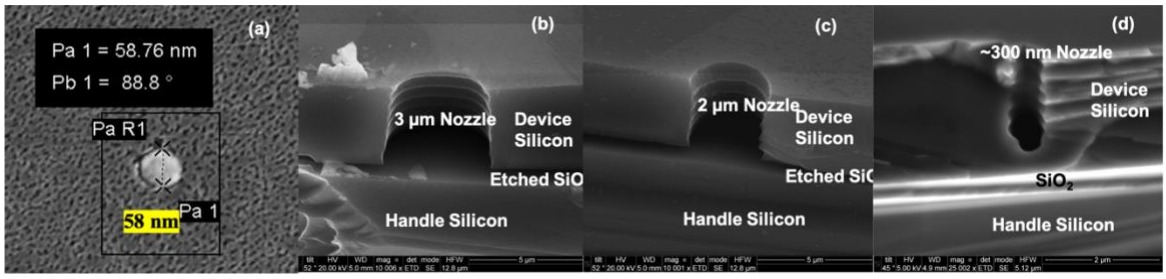

Figure 3: SEM image of nozzles etched in ~ 2 µm Si: (a) MAE for 58 nm, and DRIE for (b) 3 µm, (c) 2 µm, (d) ~300 nm.