

Field-Emission Scanning Probe Lithography-based Mix-and-Match Fabrication of Si Nanowires on SOI Substrates

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Silicon nanowires (Si NWs) are one of the most widely used low-dimensional nanomechanical structures thanks to their diverse transduction capabilities in sensing and actuation.¹ Efforts to integrate semiconductor NWs into nanoelectromechanical systems (NEMS) have intensified over the last two decades.² For this purpose, field-emission scanning probe lithography (FE-SPL) offers a cost-effective solution with single-digit nanometer resolution.³ Proximity effects are reduced by using low-energy electrons in FE-SPL and therefore it has the capability to pattern features with sub-10 nm critical dimension (CD).⁴ It was the purpose of this work to utilize FE-SPL in the fabrication of NW electromechanical switches with a CD of 10 nm (Figure 1).

FE-SPL was utilized to pattern Si NWs with different dimensions, ranging in length and width from 2 μm to 4 μm and 40 nm to 100 nm, respectively. The substrate was previously patterned with photolithography for the definition of contacts and device area. For this purpose, a silicon on insulator (SOI) substrate was used with a 9-15 $\Omega\cdot\text{cm}$ resistivity, 12 μm device layer (DL) thickness, 25 μm BOX thickness, and <100> surface orientation with DL thickness equal to NW thickness. Gate electrodes were defined on both sides of Si NW with a gap of 50 nm (Figure 1). Positive-tone patterning was carried out by utilizing AZ Barli resist followed by cryogenic reactive ion etching (RIE) of features. Isolation outside the active device area was achieved through focused ion beam (FIB) machining (Figure 2).

In this work, the performance of FE-SPL-based mix-and-match fabrication will be investigated by electrical characterization based on pull-in voltage measurements of these nanoelectromechanical switches.

¹ M. Nasr Esfahani et al. 2018 Journal of Micromechanics and Microengineering 28 045006

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³ M. Kaestner, M. Hofer, I. W. Rangelow. 2013 J. Micro/Nanolith MEMS MOEMS 12(3) 031111

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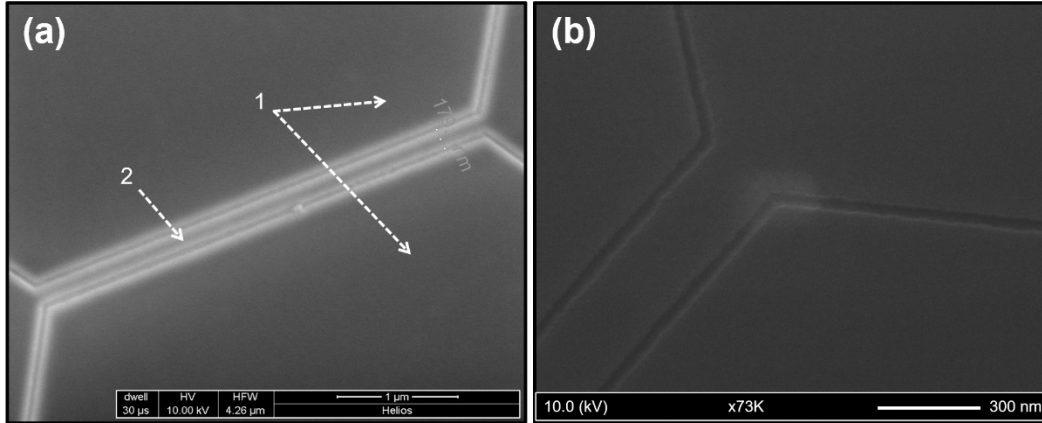


Figure 1: SEM images of a Si NW. a) Gate electrodes (1) and Si NW (2) were fabricated by utilizing FE-SPL and cryogenic RIE. b) a close-up showing one end of Si NW

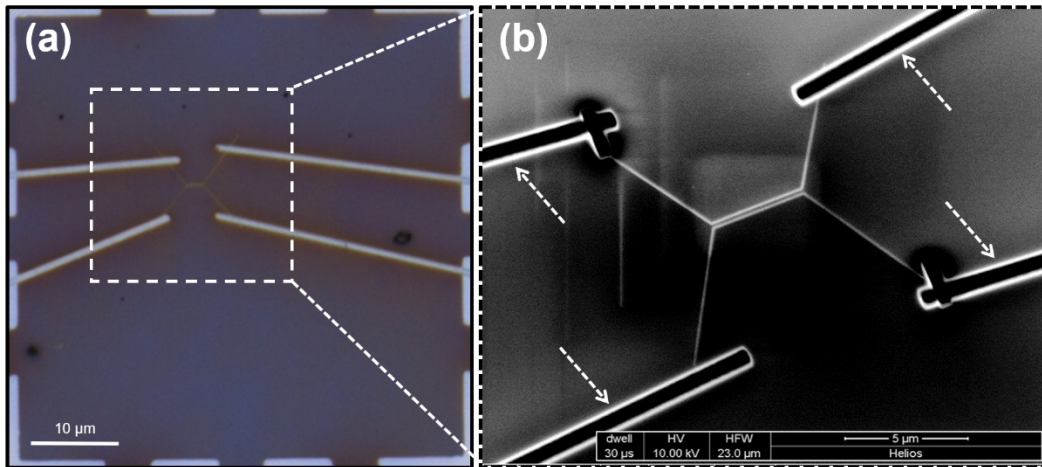


Figure 2: Images of the combination of SPL and FIB machining a) central mesa region b) a close-up SEM image on where FIB machining indicated by arrows.