

# Controlling the Etch Selectivity of Silicon using Inductively Coupled Plasma Etching with HBr

*Kun-Chieh Chien\* and Chih-Hao Chang*

Walker Department of Mechanical Engineering, The University of Texas at Austin, Austin, TX  
78712, USA

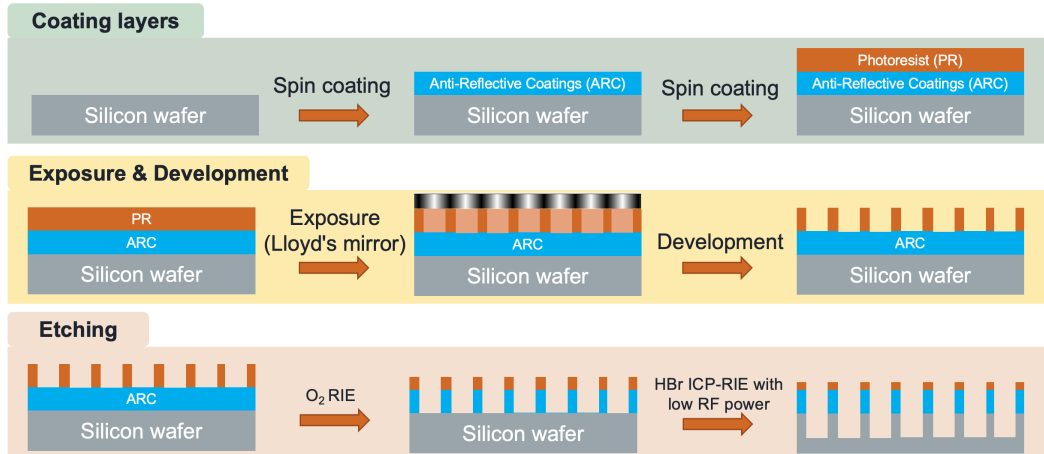
Silicon has played an important role in integrated circuits, micro-electromechanical system (MEMS), and photonics due to its superior characteristics. High aspect ratio silicon nanostructures have become more and more essential in many fields such as biosensing, photovoltaics, semiconductor, and so on. To achieve the high aspect ratio of silicon nanostructures, several techniques were introduced in the past. For example, orientation-dependent silicon wet etching,<sup>1</sup> Bosch process or silicon deep reactive ion etching,<sup>2</sup> and metal-assisted chemical etching (MACE).<sup>3</sup> Other recent techniques for hard etched materials, such as using multilayer etching mask,<sup>4</sup> might be able to provide further inspiration for fabricating high aspect ratio silicon nanostructures. However, those techniques generally include many steps and are relatively complicated.

Here, we present a simple technique, without the need for special materials, tools, and processes, for the high aspect ratio silicon nanostructure fabrication. This approach utilizes the inductively coupled plasma reactive ion etching (ICP-RIE) with the low frequency (RF) power setting to enhance the etching selectivity by favoring chemical etching.<sup>5</sup> The process of the proposed fabrication technique is illustrated in figure 1. First, a photoresist (PR) PFI-88 and antireflection coating (ARC) ARC i-CON are spin-coated on the silicon substrate. Then the PR is exposed using Lloyd's mirror interference lithography<sup>6</sup> with a HeCd laser, resulting in 1D or 2D gratings. Oxygen reactive ion etching is used to transfer the PR pattern into ARC, and HBr gas is used for the ICP-RIE process at the low RF power setting to etch the silicon substrate. After completing the ICP-RIE process, the remaining PR and ARC is cleaned by oxygen plasma etching.

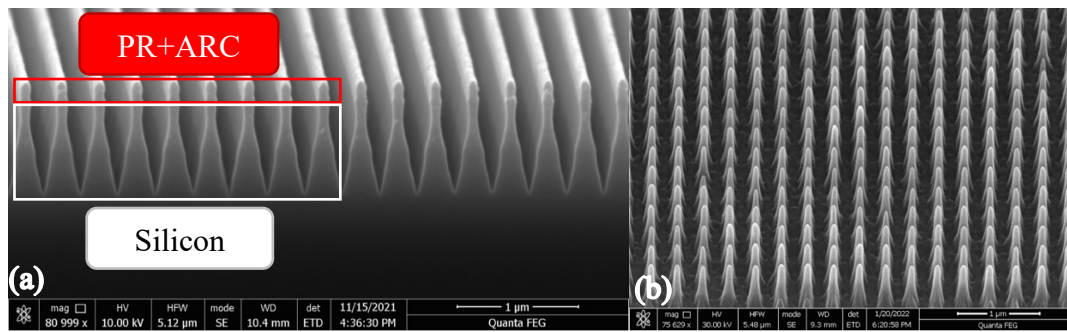
The initial results in Figure 2 show that via the low RF power setting at 15 W, high aspect ratio silicon 1D and 2D gratings can be obtained using the PR as a mask. Figure 2(a) shows the 1D silicon gratings after HBr etching, and Figure 2(b) shows the 2D silicon gratings after the oxygen plasma etching process. In Figure 2(a), The red frame shows the location of PR and ARC layers, and the white frame shows the location of silicon gratings. For the 1D gratings, the height of silicon nanostructures is around 720 nm. For the 2D silicon pillars, the height of it is around 700 nm. Both 1D and 2D silicon structures have a period of 300 nm. From Figure 2(a), we know that it is possible to achieve higher structures in the future since enough PR and ARC can be used for further etching. By the further study for the etching selectivity under different RF power settings, which is 10, 15, 30, 60, 120, and 250 W, Figure 3 shows that the etching selectivity increases exponentially as the RF power decreases. The highest etching selectivity of the current study is 36.1.

This approach demonstrates a simple fabrication process to obtain high aspect ratio silicon gratings. Those structures can be utilized in various applications such as antireflectance and their optical properties will be examined. More details will be presented including the further fabrication results, challenges, and limitations.

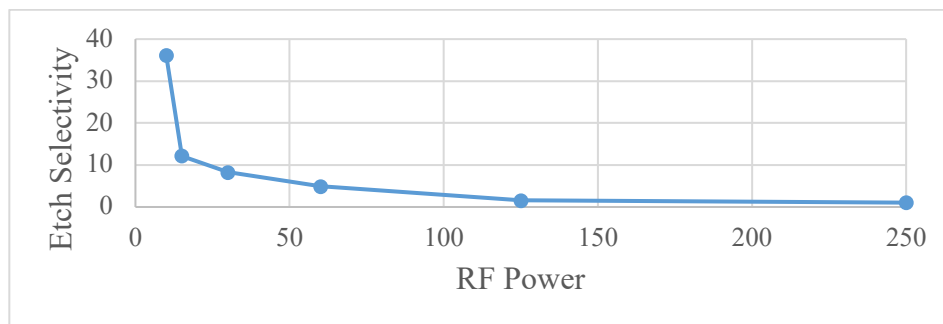
[\\*kc.chien@utexas.edu](mailto:kc.chien@utexas.edu)



**Figure 1.** Fabrication processes of proposed technique.



**Figure 2.** (a) 1D silicon gratings with 300 nm period made by HBr ICP-RIE etching at 15 W RF power. Red frame indicates the mask including the photoresist and the anti-reflective coating layers. White frame indicates the 1D silicon gratings. (b) 2D silicon pillar arrays with 300 nm period made by HBr ICP-RIE etching at 15 W RF power.



**Figure 3.** The etching selectivity of silicon over photoresist at different RF power settings.

### References:

- <sup>1</sup> S.-H. Kim, S.-H. Lee, H.-T. Lim, Y.-K. Kim, and S.-K. Lee, in *1997 IEEE 6th International Conference on Emerging Technologies and Factory Automation Proceedings, EFTA '97* (1997), pp. 248–252.
- <sup>2</sup> F. Laermer and A. Urban, *Microelectronic Engineering* **67–68**, 349 (2003).
- <sup>3</sup> Z. Huang, N. Geyer, P. Werner, J. de Boor, and U. Gösele, *Advanced Materials* **23**, 285 (2011).
- <sup>4</sup> Y.-A. Chen, I.-T. Chen, and C.-H. Chang, *J. of Vacuum Science & Technology B* **37**, 061606 (2019).
- <sup>5</sup> M. Haverlag, *J. Vac. Sci. Technol. B* **12**, 96 (1994).
- <sup>6</sup> H.I. Smith, *Physica E: Low-Dimensional Systems and Nanostructures* **11**, 104 (2001).