3D shaping of multi-layers stack using a single plasma etching step and greyscale electron-beam lithography

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This last decade greyscale lithography has been studied [1-3] to pattern 3D structure for micro-optical [4], MEMS [5], and other applications. The transfer by plasma etching, usually required has already been investigated [6] but studies have been focused on single bulk material. We present a method to shape 3D structures in a multi-layer stack by using a single plasma etching step and greyscale electron beam lithography (EBL).
The process sequence developed for the proposed technology block is shown in Fig.1(a). To calibrate the process, the associated contrast curve in negative MaN resist is measured (see Fig.1(b)). Similar to a contrast curve, a plasma etching calibration curve is determined by exposing features with different doses on the top of the stack and transferred by plasma etching during a time required to etch the full stack. After resist stripping the calibration curve shown in Fig.1(d) is measured. Based on this curve, it is possible to determine the differences doses to pattern 3D structures in the multi-layers stack Fig.1(e).
The challenge of this process is to precisely control the 3D structure shaped after a single plasma etching step in the stack. More especially for the area where the goal is to stop the etching in specific intermediate layers as illustrated in Fig.1(c) with yellow lines. Since each material has a different etch rate, the 3D resist structure needs to be precisely controlled. A slight variation in the resist thickness before the exposition or a slight variation in the etching rates of the different materials and the resist could lead to failure process. The proposed method allows a robust control of the etching step even without knowing with high precision the etching rate of every material.
In this study, we used this method to fabricate an array of TiOx resistive memory cylinder junction on top of an Al bottom electrode for the fabrication of resistive memory crossbar circuits similar to what is presented here [7,8]. The full stack is shown in Fig.1(a). The curve shown in Fig.1(d) determined the dose required to shape the 3D structure in the resist (Fig.1(c)). After plasma etching, the feature exposed at 95 µC/cm2 have been etched until the 30 nm TiN layer (Fig.1(e)). Fig.2 shows SEM images before and after the plasma etching. It demonstrates that we were able to properly shape the memory cylinders with multiple materials and the larger Al electrodes with a controlled etch stop in the thin 30 nm TiN film.

In this paper, the challenges, limitations, and robustness of the proposed method will be presented. The impact of the process variabilities like resist thickness and etch rates variations will be shown and solutions to mitigate the process sensitivity will be given. Finally, the minimum dimension that can be achieved will be presented.

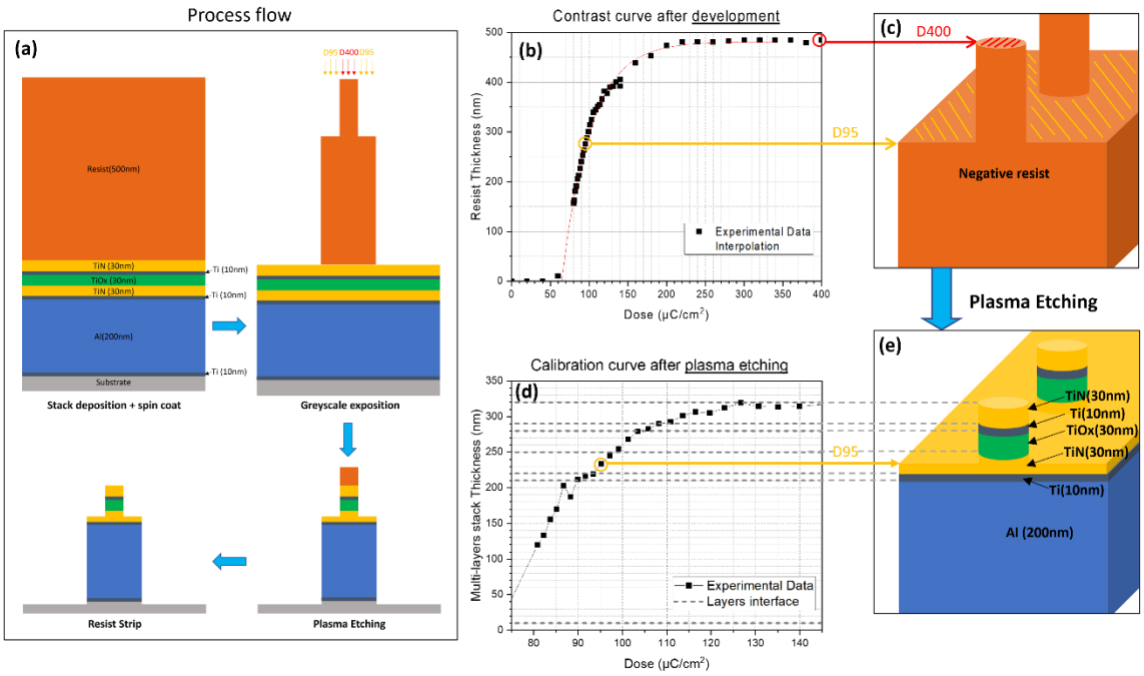

Figure 1: (a) Process flow: The Al electrode and the TiOx memory junction cylinder are shaping in a single EBL exposition and plasma etching step with a negative resist (MaN2405). (b) Contrast curve of the resist. (c) Schematic of the 3D pattern in the resist after development. (d) Calibration curve after plasma etching of the stack and the stripping of the resist. It shows the relation between the EBL exposure dose and the remaining thickness in the multi-layers stack after *270 sec* of plasma etching using BCL_3/CL_2 chemistry. (e) schematic of the final metal stack and 3D pattern after etching and resist stripping showing the very fine control of the etching stop in a thin 30 nm TiN film.

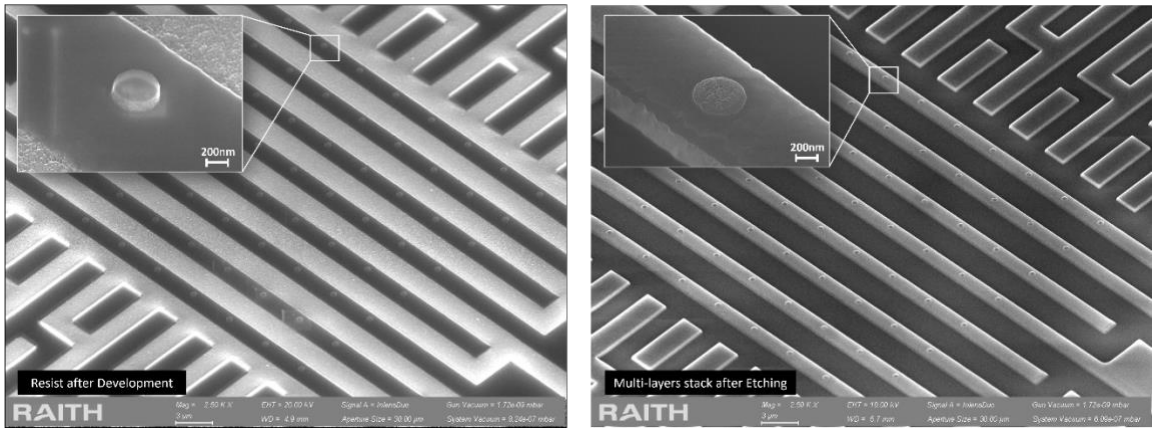

Figure 2: SEM images of bottom electrodes and TiOx resistive memory array patterned with a single etching step. *The left image* shows the fabrication step after the development and *the right image* after the plasma etching step and the resist stripping. It demonstrates that the proposed method allows very fine control of the etching stop in a thin 30 nm TiN film.

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