Challenges and opportunities of in-house integration of memristor devices on foundry CMOS

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Memristor based computing hardware needs mixed-signal functionality such as analogue to digital converters (ADCs), digital to analogue converters (DACs), encoders, decoders, and current limiting transistors to control and program the memristor matrices. Hybrid CMOS/memristor circuitry enables integrated functional electronics in a monolithic chip design.[1] CMOS/memristor circuits promise to achieve all desired properties such as high speed, low energy, high density, low cost, and high endurance.[2] However, foundry tape-outs in this hybrid technology are limited and expensive.[3] Moreover, new optimized memristor devices are being developed in academic facilities with better performance, thus requiring in-house integration with separately fabricated foundry CMOS before being suitable for system prototyping.

In this work, we discuss several challenging factors for in-house academic integration of memristors with good alignment and yield. Figure 1 shows an alignment marker and the desired monolithic integration memristor/transistor at the device level and at the chip level for 20,000 devices[4]. Fabricating memristor devices requires thin films and assumes a planar surface for optimal device behavior. CMOS chips can come from the foundry pre-planaraized, but planarization via chemical mechanical polishing using a carrier wafer is also possible.[5] A foundry-planarized CMOS chip in 180 nm technology is measured using AFM in the via regions used to connect the metal 5 lines of the selector transistor to the bottom electrode of the memristor device (Figure 2). A second challenge for nano-scale devices is aligning the memristor features during electron beam lithography. Multiple layers of the chip are separated by thick oxides and vias are the only metal structure present on the top surface of the chip. The thick oxide layer causes large charging effects when imaging with the electron beam, making it difficult to find the alignment markers. One solution is using higher accelerating voltage and aperture size. Figure 3 shows the role of the accelerating voltage and aperture size on chip imaging. The observations of this investigation can be applied to integration of other novel devices.

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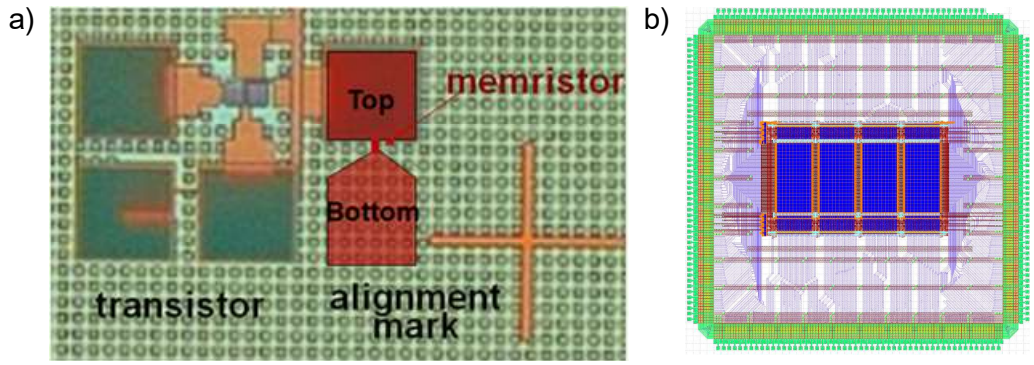

Figure 1: Proposed integration (a) 1 memristor / 1 transistor cell. (b) design for an array-level integration of 20,000 memristor devices on CMOS.

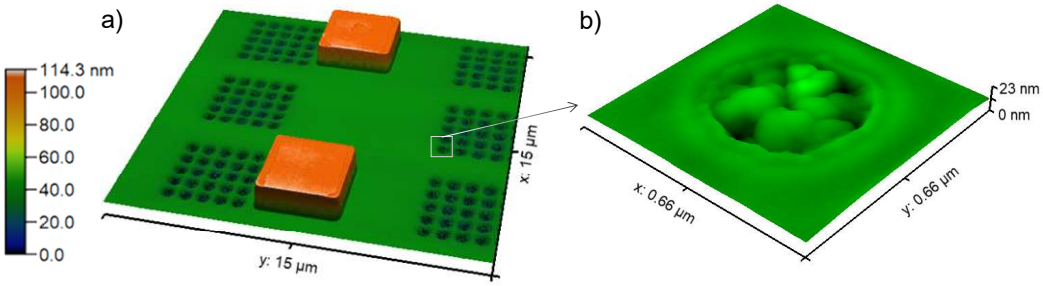

Figure 2: AFM image of the planarized chip surface of a) a single transistor's vias with metal pads added in-house (shown in orange) and b) detail of a single via showing surface roughness.

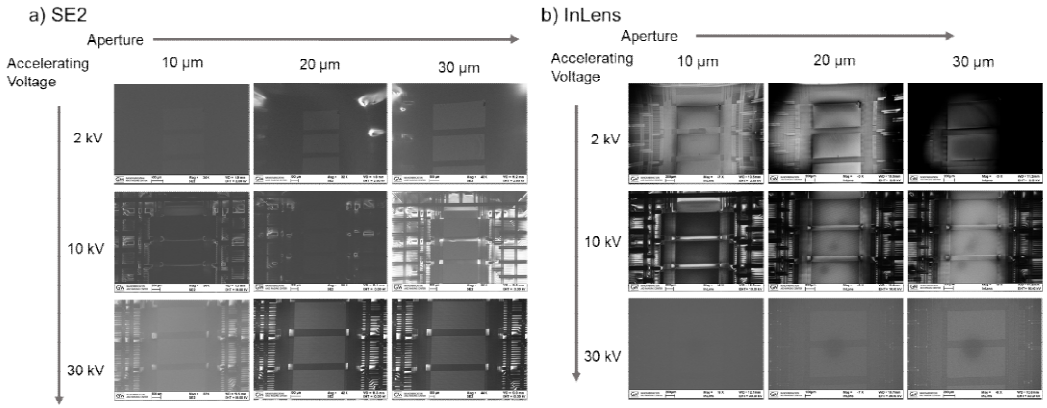

Figure 3: SEM Images from a) SE2 detector and b) Inlens detector of the CMOS surface at 2 kV, 10 kV, 30 kV accelerating voltages and 10 µm, 20 µm, 30 µm aperture size. For both detector 30 kV accelerating voltage and 30 µm aperture size are the optimum settings for imaging without severe charging and distortion. Images obtained in an entry-level electron beam lithography system.