Developing silicon MOS quantum dots with integrated plasma oxidized AlO_x SETs

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Hybrid MOS (metal-oxide-semiconductor) quantum dots with Al-based charge sensors are designed and modeled with the aim of optimizing charge sensor sensitivity while maintaining robust control of the dot chemical potential. To pursue this goal, we explore novel lithographic designs coupled with developing reliable capacitance modeling that can feedback on the lithographic design—the latter will be the emphasis of this talk. Specifically, we model the capacitance of nanodevices with Al-based SETs (single-electron transistors) integrated into the lithographic gate system of Si MOS quantum dots (see figure 1) and adjust the design rules to find the impact on capacitances for further refinement. Our group previously reported ultra-stable Al-based SETs that showed acceptable stability for use as charge sensors with MOS quantum dots by producing the charge sensor tunnel junction using plasma oxidation[1]. In that work, the total charge offset drift for Al-based SETs was $\Delta Q_0 = (0.13 \pm 0.011)$ e with significant jumps over 7.6 days, setting the stage for integration with MOS devices.

Using a combination of finite element capacitance solvers and a master equation approach, we simulate the charge sensor signal expected for a single spin readout configuration. There are two problems that we are facing: 1) we are not finding good agreement between the modeled capacitance and experimental measurements of similar devices, which may be partially due to 2) the difficulty of accurately modelling the tunnel junctions fabricated by double angle deposition, which has a complicated overlap geometry. We are currently refining the gates' structural representation in the model to improve the agreement compared to experimental results. None-the-less, using the capacitances as found thus far in the mast equation approach, we are surprised to find that good charge sensing conditions may persist to larger than expected sensor bias, rather than only at very small bias, which gives rise to the narrowest Coulomb peak broadening. Looking forward, we expect to use this modelling to optimize the design of the device's structure by iteratively changing the layout parameters before performing physical fabrication steps.

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[1] Hong, Y., Stein, R., Stewart, M.D. *et al.* Reduction of charge offset drift using plasma oxidized aluminum in SETs. *Sci Rep* **10,** 18216 (2020). https://doi.org/10.1038/s41598-020-75282-4

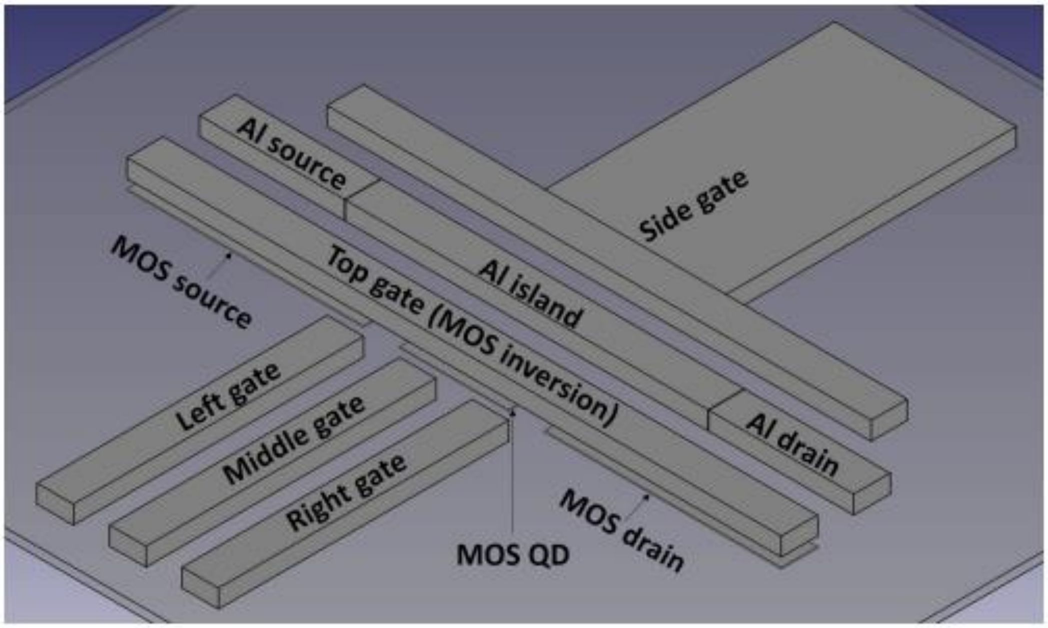

Figure 1: An example layout of the metal gate structure and the inverted electron gas in an Si MOS quantum dot device with integrated aluminum oxide charge sensors, as represented in the finite element capacitance solver package. In this case, the elements in the lower left are primary to the MOS quantum dot, and those to the upper right are primary to the AlOx charge sensor.