Markerless chip-scale fabrication of FETs by mix and match of thermal scanning probe lithography and direct laser writing

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Thermal scanning probe lithography (t-SPL), facilitated by the NanoFrazor technology, uses a heatable ultra-sharp tip for the simultaneous patterning and inspection of nanoscale structures on a surface, namely on thermal resists[1]. The technology has proven its value as an enabler of novel ultra-high resolution nanodevices[2], as well as an asset for improving the performance of existing device concepts[3]. In doing so, t-SPL is establishing itself as a mature direct-write nanolithography tool, as well as a complementary extension to other mask-less nanolithography methods such as electron beam lithography (EBL).

However, while patterning below 10 nm resolution is achievable and the writing physics would support >10x higher speeds, throughput is currently limited by distortions of the scanner motion. Towards this end, an integrated laser write head for direct laser sublimation (DLS) of the thermal resist has been introduced for the significantly faster patterning of micrometer to millimeter-scale features[4]. Remarkably, the areas patterned by the tip and the laser are seamlessly stitched together, and both processes work on the very same resist material, enabling a true mix-and-match process with no developing or any other processing steps in between.

Here, we demonstrate how the combined tip and laser patterning has been used for the first time for centimeter-sized chip fabrication of complete field effect transistor (FET) devices, with channel widths in the 15 – 50 nm range and channel heights of 60 nm (Figure 1). For patterning the gates, an automated markerless overlay algorithm correlating the device geometry with measured

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[1] S. T. Howell et al., Microsyst. Nanoeng. **6**, 21 (2020).
[2] M. J. Skaug et al., Science **359** (6383), 1505–1508 (2018).
[3] X. Zheng et al., Nature Electronics **2**, 17-25 (2019).
[4] C. D. Rawlings et al., Nanotechnology **29** (50) 505302 (2018).

sample topography is applied, enabling a fully automated and autonomous patterning process over the entire chip. This process includes the automated detection of the correct patterning position, as well as the automated on-the-fly correction of the writing position for minimal overlay errors. The t-SPL tool also allows for the prediction of the resist layer thickness to optimally adjust the writing depth. The work presented here paves the way for t-SPL's development into a fully automated, high-precision direct-write nanolithography tool with a significantly increased throughput.

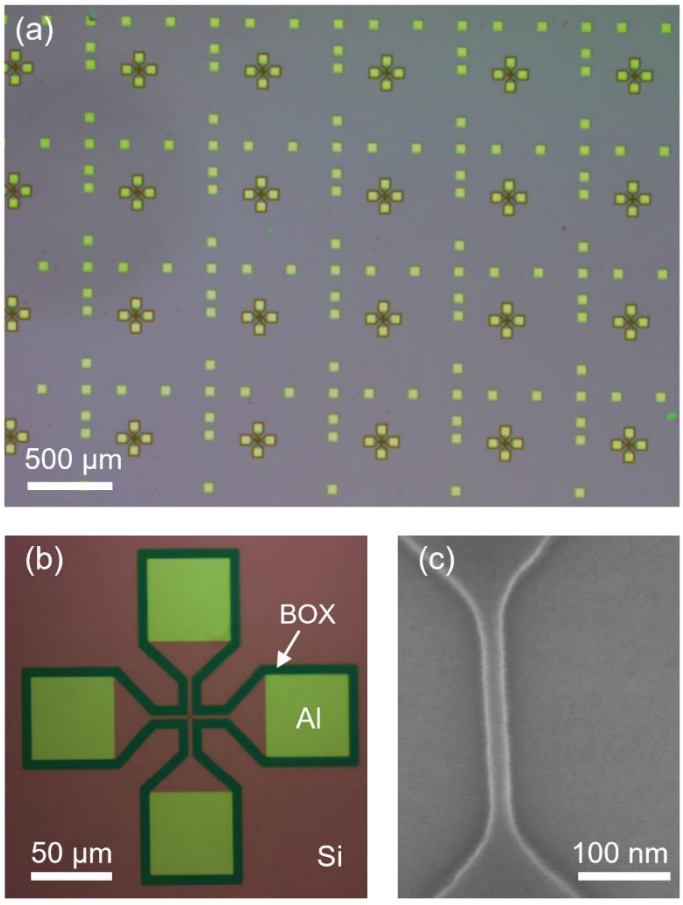

Figure 1: (a) Optical micrograph of a FET array (here without top gates) on a silicon-on-insulator (SOI) chip. The contact pads and leads were patterned by laser and the fine features by t-SPL. (b) An individual FET with Al contact pads. The exposed buried oxide (BOX) is seen as a green rim around the electrodes. (c) A scanning electron micrograph of a Si fin channel fabricated using t-SPL. The channel width is approximately 20 nm, and the fin height is 60 nm.