Microscale Additive Manufacturing of Metal Interconnects using Microscale Selective Laser Sintering

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As transistor scaling has started to reach its limits in recent years, chip designers and semiconductor manufacturers have had to look more broadly at how semiconductor system architectures are designed and assembled or "packaged," to maintain the same rate of semiconductor device performance improvement. To this end, semiconductor manufacturers have moved towards new, high-performance system architectures such as system-in-package or stacked-chip designs, where multiple different types of semiconductor devices (processers, memory, RF, MEMS, etc.) are integrated into one 3D package. This has allowed semiconductors to continue to improve in terms of both performance and efficiency, by moving processing power closer to its points of use within the package. However, these new architectures require much smaller and more complex 3D interconnect structures between the chips within the package. Current interconnect structures are generally fabricated using a multi-step process involving photolithography, etching, electrochemical deposition (ECD), and chemical-mechanical polishing steps. This approach is time-consuming and expensive, and it severely limits the size/shape of the interconnect structures that can be produced. Continued progress requires new technologies to address these problems.

Recently, we have developed a new microscale additive manufacturing process called microscale selective laser sintering (μ-SLS) that has the potential to overcome many of the current limits in advanced packaging applications, through the direct, high-throughput fabrication of 3D metal structures with feature sizes of less than 5 μm and aspect ratios of greater than 20:1. In μ-SLS, a layer of nanoparticle (NP) ink is coated onto a substrate using a slot-die coater. The resulting wafer is then shuttled to the optical subsystem using a custom air-bearing stage. There, a laser is focused through a digital micromirror device (DMD) to sinter the nanoparticles into the desired pattern. After the first layer is sintered, the air-bearing stage moves the substrate back under the coater for the deposition of the next NP layer. The process of deposition, transfer, and sintering is then repeated until the 3D part is built. The excess un-sintered ink is then removed using a solvent bath. Figure 1 shows a schematic of the μ-SLS process and the different subsystems involved. Preliminary results on the sintered parts show a resistivity of 4-5 times the bulk metal resistivity, which is competitive with the resistivity of current ECD interconnect technologies[1].

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[1] Roy, N. K., Behera, D., Dibua, O., Foong, C., and Cullinan, M. A., 2019, "A Novel Microscale Selective Laser Sintering (μ-SLS) Process for the Fabrication of Microelectronic Parts," Nat. Microsystems Nanoeng., **5**(64).

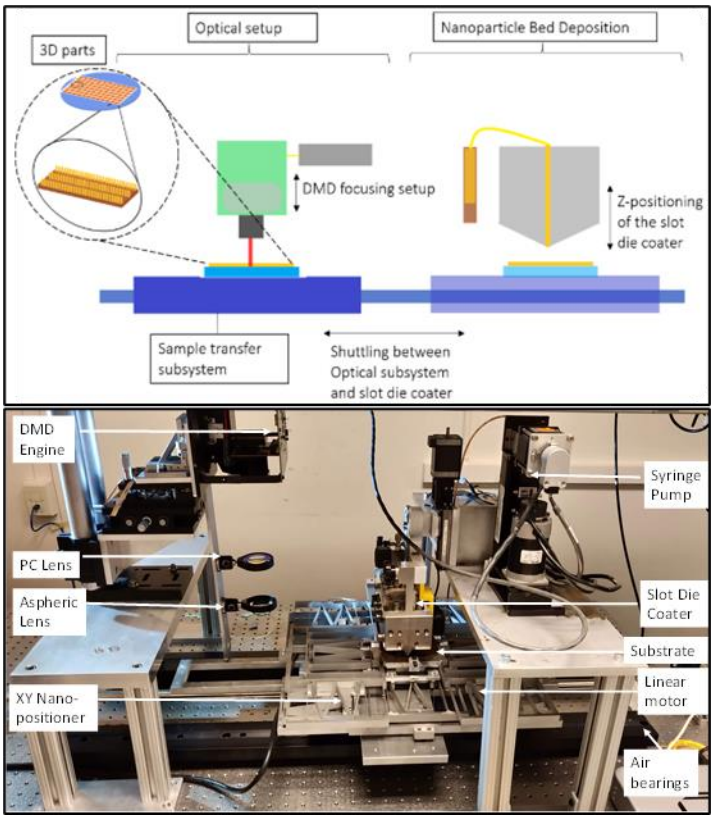

Figure 1: (Top) Schematic of the µ-SLS process, (Bottom) Picture of the actual µ-SLS tool

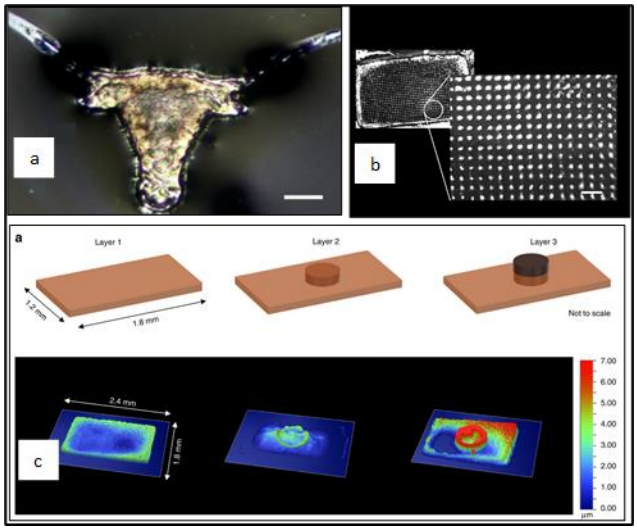

Figure 2: (a) Sintered Longhorn logo (scale 100 µm). (b) Sintered circular pillars of 20 µm diameter and 40 µm pitch (scale 80 µm). (c) Schematic and profilometer images of the progression of a 3-layer sintering process