Multilayer superconducting fabrication process for microwave and digital electronics

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Superconducting nanowires have attracted interest from researchers in high energy physics and quantum information systems due to their high kinetic inductance[1], ability to drive high impedance loads, low power, and direct integration with superconducting nanowire single-photon detectors (SNSPDs). These properties can be leveraged in the design of compact microwave circuits or SNSPD readout integrated circuits. In either case, the development of a robust multilayer fabrication process compatible with superconducting thin films is required [2].

We present a multilayer fabrication process using thin film niobium nitride (NbN) and plasma enhanced chemical vapor deposition silicon dioxide (PECVD SiO_2) as electrical isolation between superconducting and normal metal layers. Both positive and negative tone electron beam lithography processes were used to pattern specific layers. For the positive tone process, we used ZEP530A with an applied dose of 550 $\mu C/cm^2$. For the negative tone process, we used 6% dilution of hydrogen silsesquioxane (HSQ) and a dose of 4000 $\mu C/cm^{2.}$. Reactive ion etching in a carbon tetrafluoride (CF_4) atmosphere at 50 W was calibrated to etch NbN at a rate of 5nm/min and PECVD SiO_2 at a rate of 10nm/min. For normal metal layers the positive tone process was used to lift off a 50 nm layer of gold and a 5 nm titanium adhesion layer.

To investigate the ability to yield microwave circuits we fabricated tunable microstrip resonators. The fabricated resonator had a quality factor of ~ 200 which is primarily limited by the SiO_2 dielectric used in this work. The resonant frequency could be tuned from 800 MHz to 300 MHz by increasing the inductance as a function of heater current.

Fabricating large digital circuits using nanowires will require integrated multilayer interconnects. To assess the fabrication yield of this multilayer process, chains of superconducting vias were fabricated. The superconducting critical current (I_c) as a function of the number of vias in the chain was measured, showing a small decrease in the I_c as the number of vias increased.

The fabrication process presented can be used for the design of other microstrip circuits, superconducting memories, and digital nanowire circuits. Such devices would allow for integrated signal processing and digital logic for SNSPDs and superconducting qubits.

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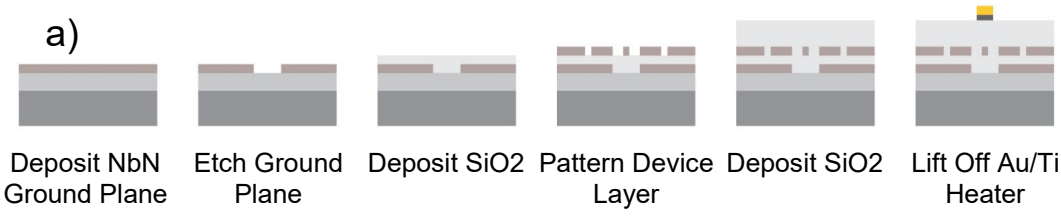


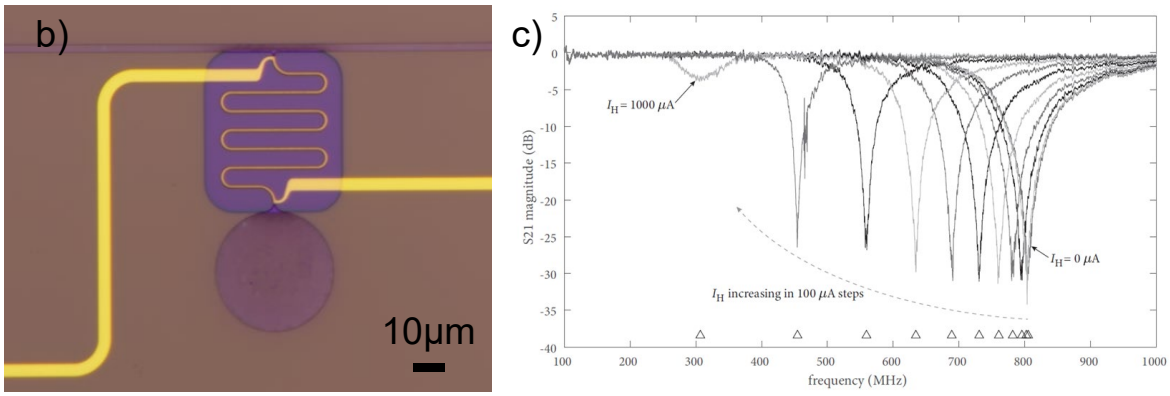
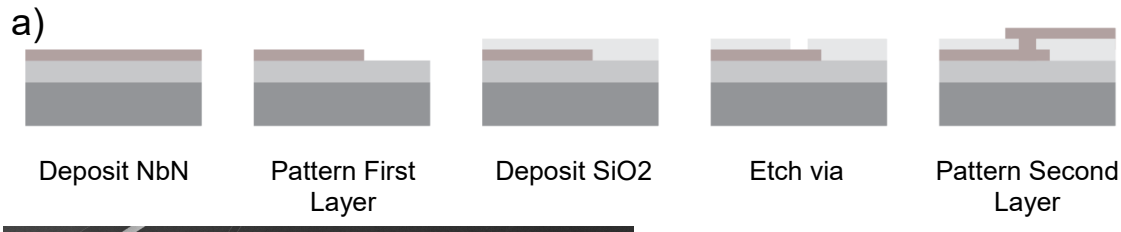


Figure 1. a) Layer stackup of the fabrication process. b) Optical micrograph of a tunable superconducting microstrip resonator. c) S21 magnitude up to 1GHz showing a decrease in the resonant frequency as a function of heater power.



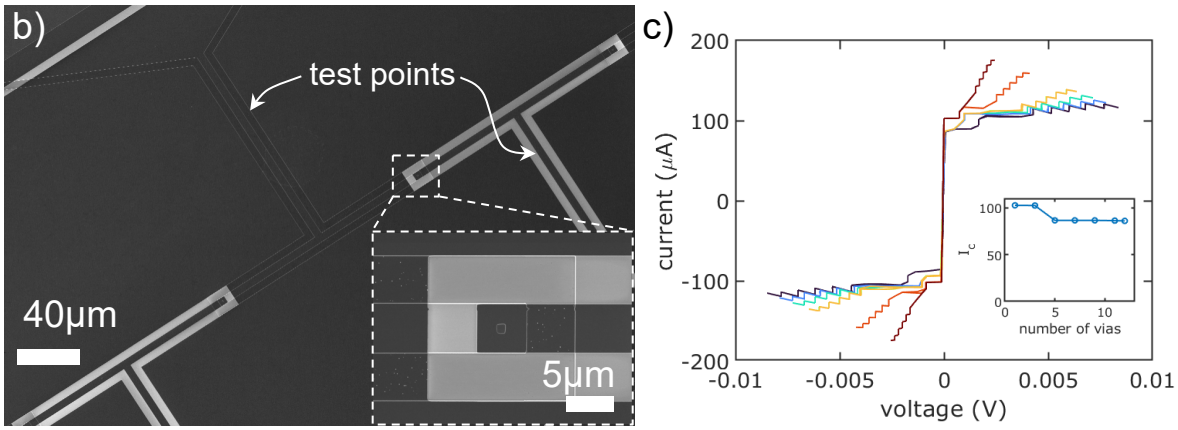


Figure 2. a) Layer stackup of the fabrication process. b) Scanning electron micrograph of a superconducting via chain. Test points are located between two vias on alternating layers. c) IV characteristics of a chain of 1-12 vias. The inset shows the measured critical current decreases as the number of vias increase due to the material/fabrication defects.