## Controlled line edge roughness for novel nanodevice fabrication with the NanoFrazor

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The NanoFrazor uses thermal scanning probe lithography (t-SPL) for the simultaneous patterning and inspection of nanoscale structures<sup>1</sup>. The technology has proven its value as an enabler of novel ultra-high resolution nanodevices<sup>2</sup>, as well as an asset for improving the performance of existing device concepts<sup>3</sup>. In doing so, t-SPL has established itself as a direct-write nanolithography method for advanced nanofabrication. The technique employs a heated ultrasharp tip to locally remove thermal resists or modify surfaces, while remaining non-invasive towards sensitive materials and free from proximity effects.

A broad range of t-SPL applications<sup>1</sup> spanning from ultra-high resolution 2D and 3D patterning to chemical and physical modification of matter at the nanoscale have been demonstrated in the last few years. Applications such as critical areas of nanoelectronic devices and waveguide structures are gaining significance with advances in fabrication technology. The key strengths of the NanoFrazor relevant for these applications include nanometer-precise markerless overlay, and the ability to minimize line edge roughness (LER) in the resulting structures. Such properties are crucial for enabling the fabrication of novel nanodevices with emerging 2D materials, as displayed in Figure 1. The NanoFrazor tool allows for the control of LER in an on-the-fly manner by adjusting the pixel size during patterning. In Figure 2, we show that for written pixel sizes of 10 nm in a thermal resist, the LER of the final pattern transferred into silicon is below 3 nm.

A further distinct property of the NanoFrazor technology is the capability to pattern in 3D with vertical resolution of a single nanometer. With this ultra-precise grayscale lithography ability, novel applications in photonics have been demonstrated, such as custom-made optical Fourier surfaces<sup>4</sup>, as seen in Figure 3. These applications require precise control of pixel sizes for pattern fidelity, similar to the LER control studied for waveguide structures.

In this talk, the background, and unique capabilities of the NanoFrazor technology will be discussed. Key applications enabled by this technique combined with LER control will be highlighted, such as the fabrication of novel electronic devices based on 2D materials, and the new advances in t-SPL enabled photonics devices.

<sup>&</sup>lt;sup>1</sup> S. T. Howell et al., Microsyst. Nanoeng. **6**, 21 (2020).

<sup>&</sup>lt;sup>2</sup> M. J. Skaug et al., Science **359** (6383), 1505–1508 (2018).

<sup>&</sup>lt;sup>3</sup> X. Zheng et al., Nature Electronics **2**, 17-25 (2019).

<sup>&</sup>lt;sup>4</sup> N. Lassaline et al., Nature **582**, 506-510 (2020).



*Figure 1:* A typical application of NanoFrazor lithography is the fabrication of high-resolution metal contacts using lift-off on novel 2D materials. Here, in-situ NanoFrazor topography imaging is utilized to locate monolayer molybdenum disulfide (MoS<sub>2</sub>) flakes and directly pattern metal electrodes onto them, without the need for markers. In this way, ohmic contacts have been fabricated on monolayer MoS<sub>2</sub> flakes, without causing any damage to this sensitive material<sup>5</sup>.



*Figure 2:* (a) - (d) SEM micrographs of t-SPL waveguide patterns written with different pixel sizes, from 40 nm pixel size in (a) to 10 nm pixel size in (d) and transferred via reactive ion etching (RIE) into a silicon substrate. The line edge roughness of the final pattern in silicon is tuned by controlling the initial pixel size of the pattern during t-SPL writing. Scale bar is 500 nm. (e) Variation of the line edge roughness of the waveguide etched into silicon according to the t-SPL writing pixel size. For a pixel size of 10 nm, a final line edge roughness of less than 3 nm is achievable.



*Figure 3:* NanoFrazor grayscale lithography with sub-nm precision enable new applications in photonics. Scanning electron microscope (SEM) images of: (a) an 8-level hologram pattern written with t-SPL on a thermal resist and etched into silicon with reactive ion etching (RIE)<sup>6</sup>, (b)-(c) optical Fourier Surfaces made in Ag (and other materials), allowing for free and clean combination of sharp selected frequencies<sup>7</sup>. Scale bar: (a) 500 nm, (b)-(c) 3  $\mu$ m.

- <sup>5</sup> X. Zheng et al., Nature Electronics **2**, 17-25 (2019).
- <sup>6</sup> T. S. Kulmala et al., Proc. SPIE **10584**, 1058412 (2018).
- <sup>7</sup> N. Lassaline et al., Nature **582**, 506-510 (2020).