# An Experimental Study of the Effect of Mask Morphology on Very-Large Area Graphoepitaxy of InP on Silicon Enabled by Nano-imprint Lithography

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InP is an extremely important material resulting from its superior electron velocity, which is widely used in the fields of optoelectronic device manufacturing, high-speed electronic device preparation, and the photovoltaic industry. Achieving large-area, ultra-fast and high-quality growth of InP is an ongoing pursuit. The existing methods of growth of InP on Si substrate relied on buffer layers to mitigate the lattice mismatch or graphoepitaxy through high-aspect-ratio openings achieving the continuous film. However, the buffer layer resulting in a distant separation between the substrate and InP layer, which severely limits the device performance [1,2]. The excessive cost and time-consuming fabrication of a large-area (>1000μm$^2$ ) mask prevent the graphoepitaxy from being widely used. It also hinders the systematic study of the effect of mask morphology on graphoepitaxy. Nanoimprint lithography (NIL) perfectly overcomes these shortcomings enabling the study of the effect of mask morphology on growth of InP, such as geometry of sidewall and strip orientation systematically.

Through NIL and RIE, large-area high-aspect-ratio mask openings are easily patterned onto the lattice mismatched substrate. Graphoepitaxy requires careful control of the geometry of the sidewall leading to suppression of defect propagation and ensuring uniform growth. We intentionally fabricated sample with different sidewall as shown in Figure 1a & 1b. The vertical side wall (figure 1a) was found to be hard with the continuous growth of InP. It provides far more anisotropic openings compared with the structure shown in figure 1b, however, vertical sidewall is accompanied by a thick passivation layer, as well as unavoidable contamination from the etching process. Reproducible high-qualtiy graphoepitaxy was achieved based on the undercut sidewall. The resulting strucutre is shown in figure 1b. At the cost of the sidewall geometry, the passivation layer and contamination were completely ellimintaed resulting in improved reproducible InP film. Once the InP has grown out of the openings, the InP growing out of adjacent openings are required to merge seamlessly. Coalescence phase demonstrates a strong dependence in morphology on orientation. In figure 2, top view SEM of eight coalesced arrays of stripes are presented. The opening orientation varied from 20° to 80°. The smooth film occurs with an originating stripe orientation 60°-off.

The IV characteristics of PN junctions fabricated on the InP film are measured. The mesa junction used for electrical characterizations was fabricated through graphoepitaxy enabled by NIL, as shown in figure 3a. The IV curves are presented in figure 3b. The most noticeable feature of the IV characteristics is that the coalesced film has a larger current, as well as lower resistance than film grown on buffer layer, which means defects formed owing to lattice mismatch can be effectively removed and films coalesced faultlessly and smoothly. By applying NIL to graphoepitaxy, the effect of mask morphology on formation of single-crystal films of InP on Si was systematically studied which paves the way for the monolithic integration of similar materials such as InGaAsP and InGaAs onto lattice-mismatched substrate.

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† These authors contributed equally to this work.

1. A. W. Poon et. al., Proc. of SPIE **8628** (2013)
2. A. Joshi and G. H. Olson in: *Handbook of Optics* 2nd ed (Optical Society of America, 1995) Chapter 16

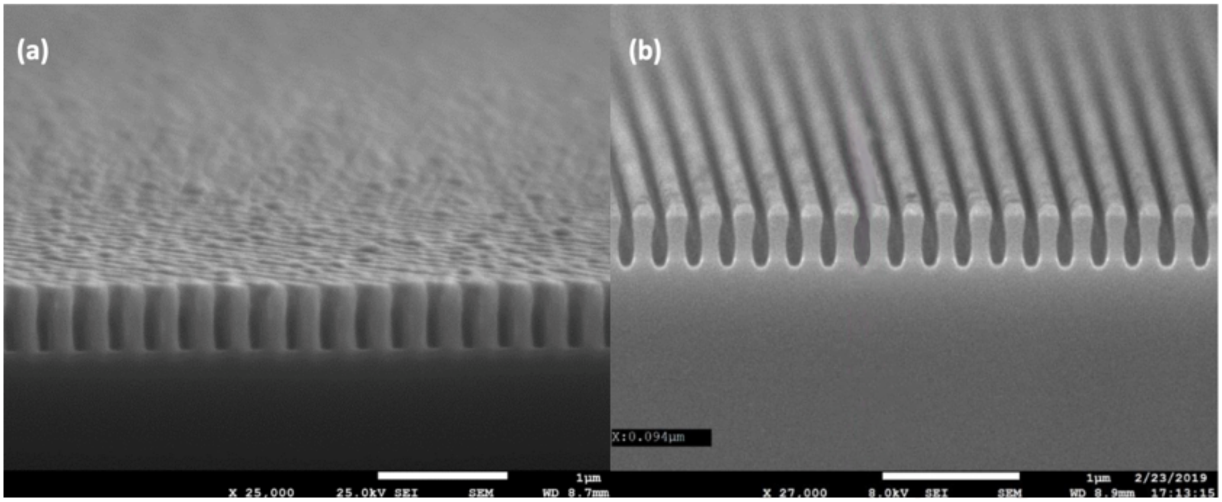



Figure 1. Cross-section view SEM images of NIL mask. (a) The anisotropic, deep, high-aspect ratio openings with vertical side wall. (b) Undercut sidewall to improve the reproducible selective growth.

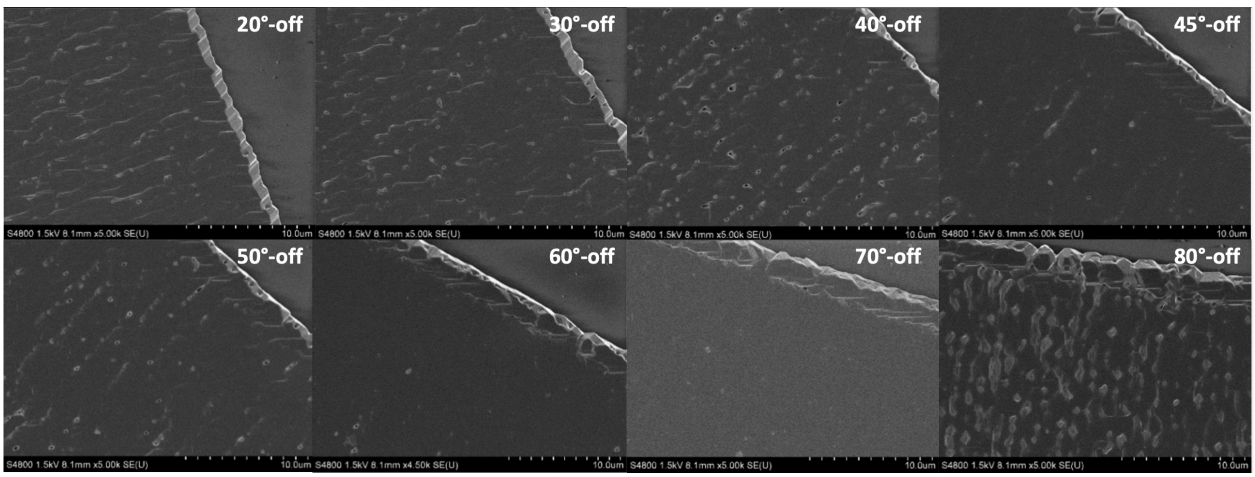
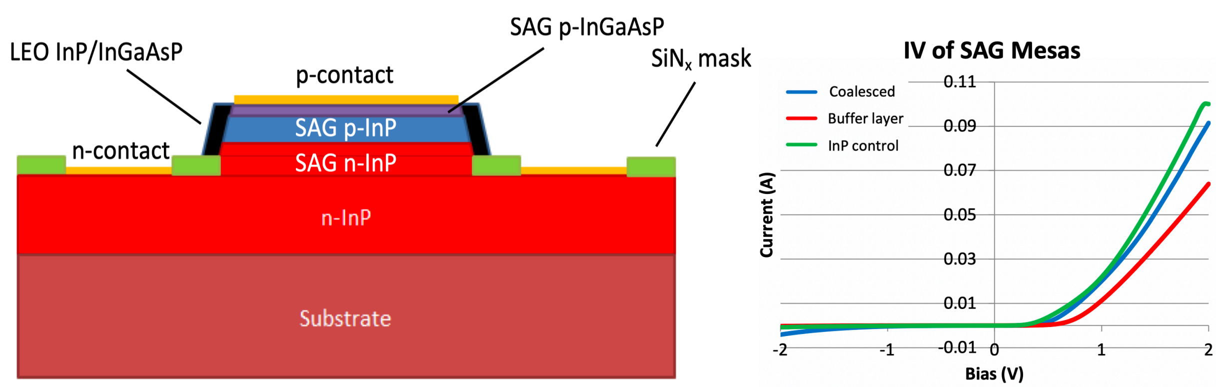



Figure 2. Dependence of film morphology for coalesced stripes with varying orientation. The opening orientation varied from 20° to 80°. Only stripes near 60°-off coalesced seamlessly. For the rest of orientations, there are countless defects.




(a) (b)

Figure 3. (a)The design of Mesas junction used for IV measurement fabricated by NIL enhanced SAG. (b) IV curve of SAG Mesas.