Edge-contact MoS_2 transistors fabricated using thermal scanning probe lithography

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Two-dimensional materials (2DM) have emerged as potential candidates for low power electronics, optoelectronics, and sensing.[1] The fabrication of devices based on 2DM using conventional lithography methods involves chemical and physical processes which produce detrimental effects on the device performance.[2,3] Additionally, the characteristic Schottky barrier appearing at the junction between a 2DM and a 3D metallic contact remains a limiting factor in the performance of 2DM-based electronic devices. When 2DM are exposed to air, molecules adhere to the surface forming layers with a thickness that can be of the same order of the 2DM itself, affecting the 2DM-metal interface in top-contact devices. Besides, 2DM have a large conductivity anisotropy between the in- and out-of-plane directions. This means that, in multilayer devices, when top-contact configuration is used, each interface between two layers acts as a tunneling barrier, decreasing the final performance of the device. In contrast, edge-contact devices enable shorter bonding distances and covalent bonding to every layer but at the expense of a more complex fabrication process.[2]

Here, we propose a process based on thermal scanning probe lithography (t-SPL) to fabricate edge-contact 2DM transistors (see Fig. 1).[3,4] It has already been demonstrated that t-SPL is a better candidate than electron beam lithography for the fabrication of top-contact 2DM-based field effect transistors (FETs) as the use of electrons is avoided and the heat from the tip remains sufficiently far from the 2DM, limiting the possible degradation of the 2DM properties.[5] Here, we go one-step further and achieve edge-contact by combining t-SPL with Ar^+ milling and physical vapor deposition (PVD) in the same chamber,[6] achieving a clean edge contact.

The proposed process is schematically shown in Fig. 1a and carried-out as follows. MoS_2 flakes are mechanically exfoliated onto Si substrates covered by a 200 nm SiO_2 layer. For the fabrication of the contacts, a bilayer of PPA (30 nm)-PMGI (80 nm) is used. Patterning is performed by a mix-and-match approach combining t-SPL for the small features and direct laser writing for large features, both implemented using the same commercial tool. After wet etch in TMAH solution, the samples are placed into the PVD chamber where Ar^+ milling is used to etch the flakes and, subsequently, the electrode material is deposited without breaking the vacuum. After the final lift-off, edge-contact FETs are obtained.

A set of devices with different 2DM thicknesses are fabricated. The electrical characterization shows that multilayered devices achieve a highest on/off ratio of 10^8, which is comparable to the highest reported values for MoS_2 transistors without hBN encapsulation.[6] As compared to monolayer devices, multilayer FETs show higher mobility, higher on-state current and lower contact resistance. For the sake of comparison, top-contact devices are also fabricated following a similar process but without ion milling. Top-contact devices show poorer performance compared to edge-contact ones, which is attributed to the cleaner interface between the 2DM and the metal electrode as well as a more efficient injection of the current in the later, enabled by the contact of the electrode material to every single layer of the MoS_2.

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2. Matsuda, Y. et al., *J. Phys. Chem. C* **114**, 17845–17850 (2010).
3. Conde-Rubio et al., *MicroNanoEngineering MNE conference 2021, Torino (Italy).*
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5. Zheng. et al., *Nat. Electron.* **2**, 17–25 (2019).
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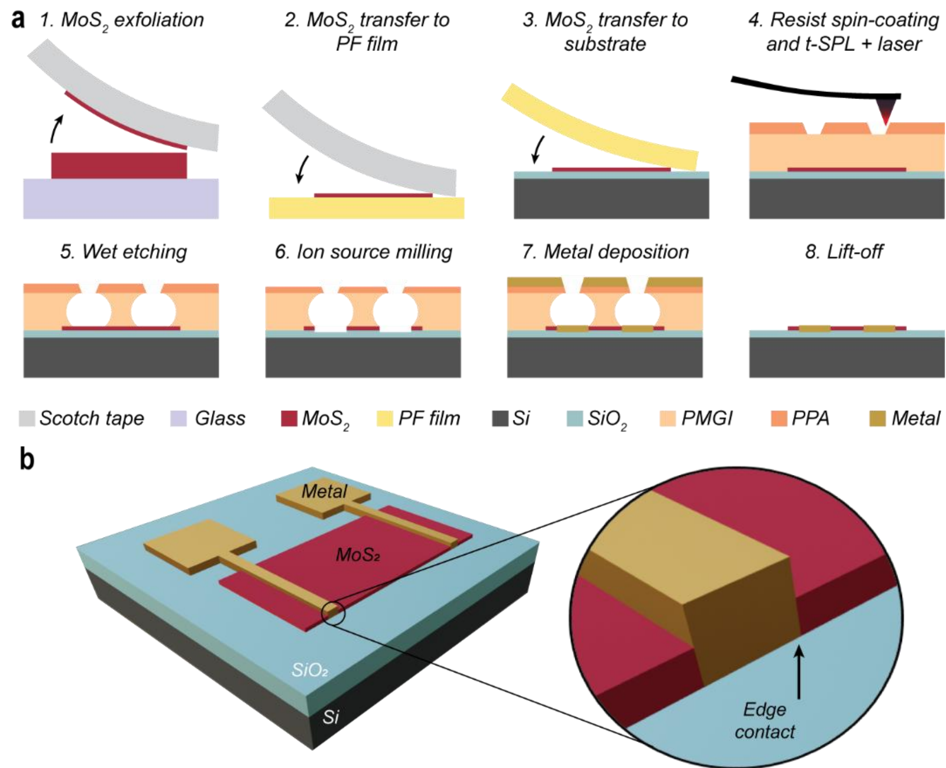

Figure 1. a) Scheme of the fabrication process, b) schematic illustration of the edge contact device.

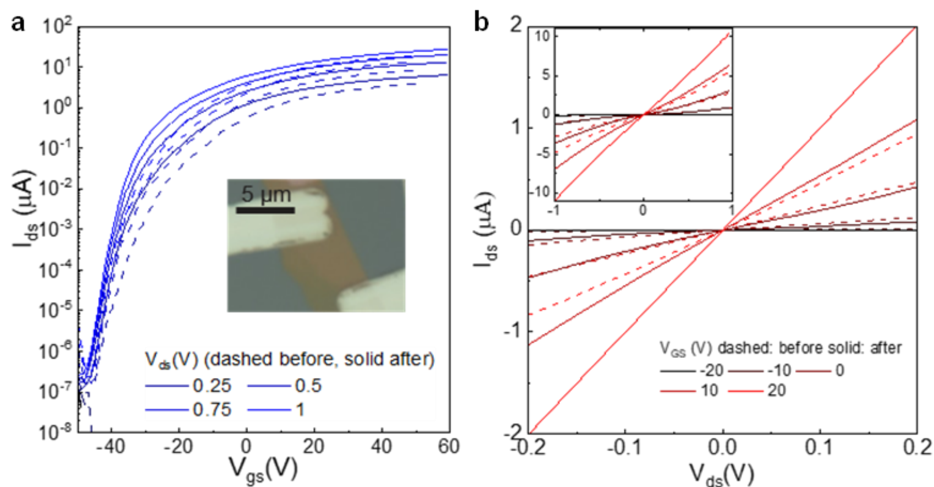

Figure 2. Electrical performance of multilayered MoS_2 edge-contact FETs, measured in air, before (dashed lines) and after (solid lines) thermal annealing at 250 ºC for 3h. The transistor's channel has a width of 4.5 µm, a length of 4.9 µm and a thickness of 6 nm. (a) Drain current, I_{ds}, as a function of the gate voltage, V_{gs}, for different values of the drain-to-source bias voltages, V_{ds}. The inset shows an optical microscope image of the device. (b) I_{ds} as a function of V_{ds} for different V_{gs}.