Nanofabrication approach for Next-Generation High-Performance FinFET Technology

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Currently, FinFET and ultra-thin-body silicon-on-insulator (UTB-SOI) are trending and expected to revolutionize the electronics future generation technology node [1]. For high mobility transistors, the epitaxial germanium on a silicon substrate (Ge-on-Si) could be a leading contender and instant solution for the next generation processing nodes as silicon technology is already well established. The Ge on insulators (GOI) production is neither profitable nor process compatible as compared to the production of SOI with Smart-Cut technology [2]. In this regard, we propose the facile cost-effective 4-layer electron-beam lithography (EBL) based processing protocols for 20 nm Ge FinFET structures on a silicon substrate, Fig. 1.

To achieve this the robust resist resolution limit for next-generation lithography down to 20 nm or below requires the resist to attain high resolutions features, low line edge/width roughness and high etch selectivity for pattern transfer. The inhouse formulation of Polymerization of (4-(methacryloyloxy)phenyl)-dimethylsulfoniumtriflate (MAPDST) negative tone resist for electron-beam lithography (EBL) and extreme ultraviolet lithography (EUVL) exposures to achieve 20-nm line patterns with good etch resistance for pattern transfer protocols are used [3] [4]. First, we investigated the properties of a specially formulated MAPDST resist which can be spun as sub 100 nm to achieve high resolution. Then sub 30nm lines with pitch down to 100nm are exposed with EBL exposure dose test. The SF_6/O_2 based reactive ion etch process is developed to transfer the MAPDST resist pattern on Ge-on-Si layers. Well resolved sub 30nm Fin structures successfully transferred on Ge-on-Si substrate, Fig. 2. Finally, a complete $Ge_{-on-}Si$ based FinFET process is developed and characterized for the realization of a 120 nm to 20nm array of FinFET devices.

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References

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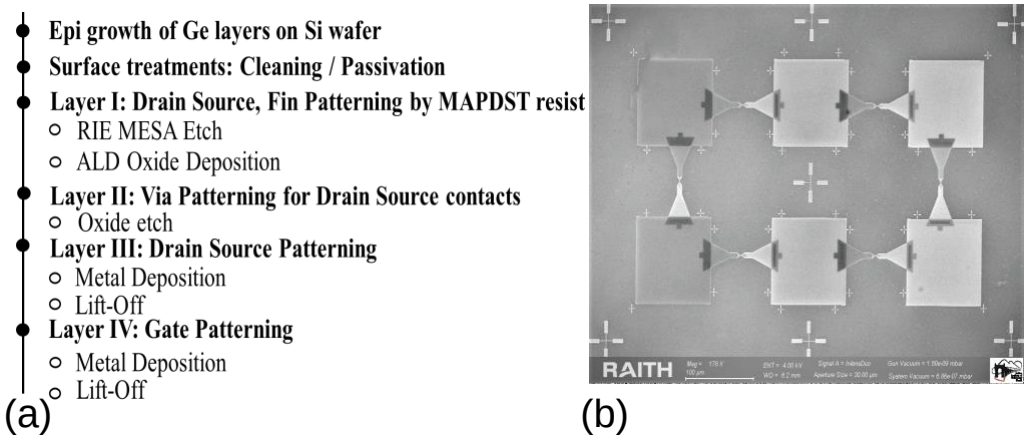

Figure 1(a): Proposed Ge-on-Si FinFET process flow. Figure 1(b) The Array of Ge-on-Si FinFETs MESA transferred on epi Ge layer with Fin widths of 120nm to 20nm.

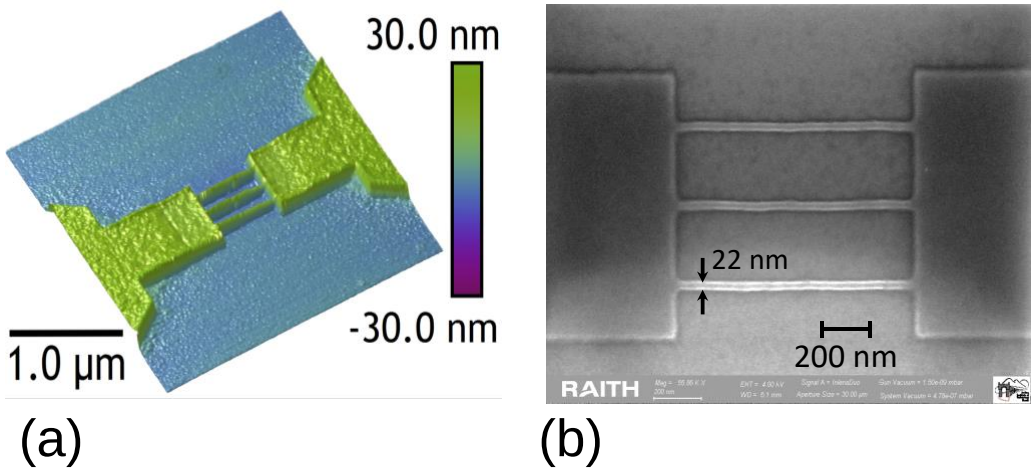

Figure 2(a): 3D AFM profile image demonstrating the of Ge channel fins transferred by Reactive Ion Etching on epi-Ge layers. Figure 2(b) depicts the Fin width of 22nm with a pitch of 100nm.