Multiplexing Rubbing-Induced Site-Selective (RISS) Production of Bi_2Se_3 Based Memristive Devices

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Bismuth selenide (Bi_2Se_3) has attracted huge attention as a quasi-2D layered material, potentially for making topological insulator (TI) and thermoelectric devices. [1-4] Recently it was reported that Bi_2Se_3 heterostructures processed with oxygen injection exhibit a resistance switching (RS) behavior, revealing its potential as a memristive material. [5,6] Pristine few-layered Bi_2Se_3 flakes are usually fabricated by mechanical exfoliation from bulk ingots or chemical vapor deposition (CVD) methods.[7] However, to manufacture large arrays of Bi_2Se_3 nano/microscale devices, resist-based lithography and plasma etching have to be performed on such fragile layered materials, generating detrimental contaminations and damages. In addition, the current standard cleaning methods for nanofabrication (e.g., piranha cleaning) can hardly eliminate such lithography-introduced contaminations without causing serious damages to the device features. Such lithography-introduced contamination could greatly compromise the electrical and mechanical properties of the devices and degrade the device-to-device consistency or uniformity in the arrays. Our previous work demonstrated a rubbing-induced site-selective (RISS) method capable of generating arbitrary MoS_2 patterns with no need of additional lithography or etching processes.[8,9] To further generalize the RISS process for producing Bi_2Se_3 device arrays, additional nanomanufacturing research is needed to obtain working Bi_2Se_3 device arrays.

In this paper, we report our recent progress in leveraging the RISS technology to realize site-selective growth of Bi_2Se_3 features. We further report the memrsitive switching behavior observed from the resistors made from such RISS-produced Bi_2Se_3 channels, which reveals the potential of RISS-produced Bi_2Se_3 in the application fields related to neuromorphic devices.

Our current multiplexing RISS process includes two main steps: (i) rubbing a substrate with a template bearing a pillar array to pre-define the locations and patterns of target Bi_2Se_3 device features on the substrate; (ii) site-selective CVD growth of few-layered Bi_2Se_3 patterns at the designated locations rubbered by the pillars template. **Fig.1(a)** shows the schematic illustration of a rubbing template, and **Figs. 1 (b) and (c)** illustrate the basic RISS procedure for generating an array of Bi_2Se_3 features on the target substrate. **Fig.**2 (a) and **(b)** show the optical micrograph of a representative array of RISS-produced L-shaped Bi_2Se_3 features and an as-fabricated memristor array, respectively. **Fig.3** plots the pulse-programmed characteristic curve measured from a representative Bi_2Se_3 memristor.

This work presents a novel nanomanufacturing method for fabricating Bi_2Se_3 memristor arrays and shows the potential for site-selectively growing other 2D layered materials.

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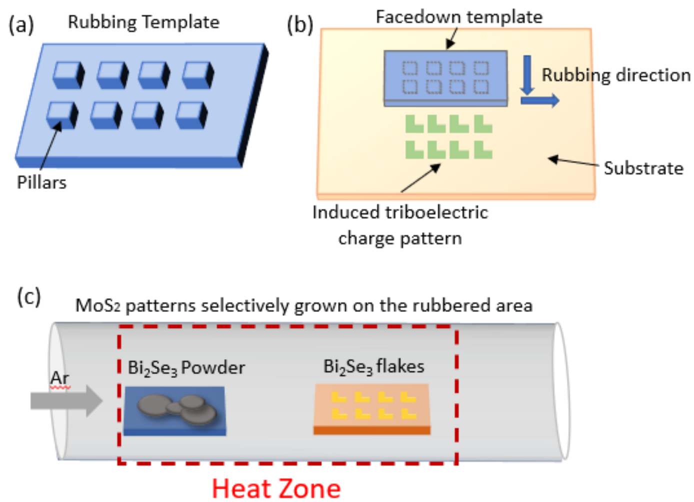

Fig.1 Schematic illustration of the multiplexing RISS method for site-selectively growing an array of Bi_2Se_3 pattern on the target substrate. (a) Schematic of a rubbing template. (b) Rubbing procedure for generating triboelectric charge. (c) CVD growth of an array of Bi_2Se_3 features.

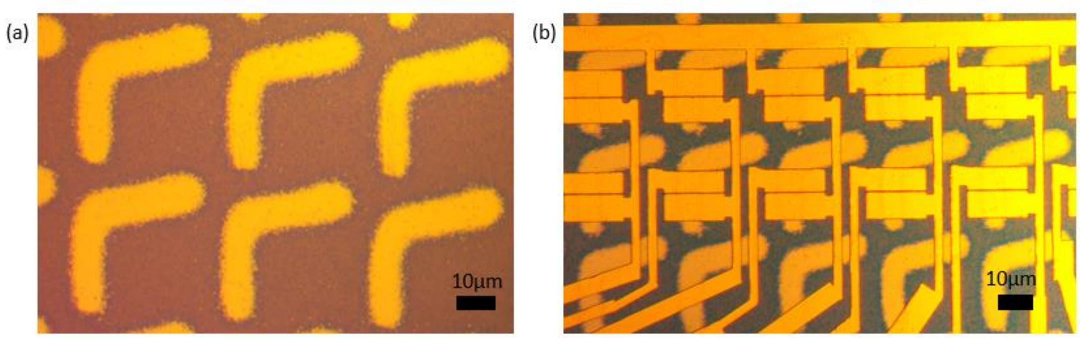

Fig.2 Optical micrograph of a representative array of (a) L-shape RISS-produced Bi_2Se_3 and (b) as-fabricated Bi_2Se_3 memristor with period of 80 µm. (Scale bar: 10 µm)

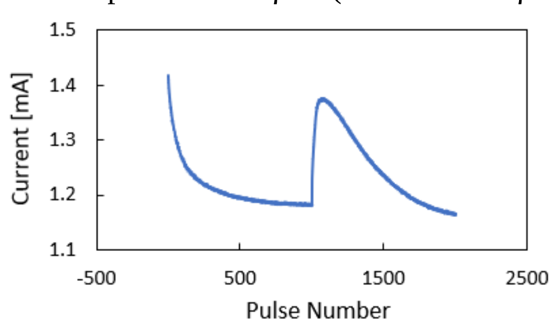

Fig.3 Measured channel current (I) versus pulse number (n) of a representative Bi_2Se_3 memristor under 5V bias.

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