Scalable Nanoimprint Manufacturing of Multi-layer Metasurfaces for Compact Polarimetric Imaging System

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Metasurface structures are attractive in broad optical applications, as they can efficiently manipulate the light propagation direction, speed, intensity, and phase. For example, we have demonstrated an ultra-compact polarimetric imaging system by utilizing double-layered metasurface structures to characterize linearly polarized light (LPL) and circularly polarized light (CPL) for full-Stokes analysis (Fig. 1a) [1]. However, the fabrication relied on electron beam lithography (EBL), which is very expensive for scalable production. In addition, stacking multiple layers of nanostructures introduced surface roughness and optical loss.

To overcome those issues, we developed a multi-functional-direct-NIL (MFD-NIL) process as a scalable manufacturing approach to integrate multiple layers of metasurfaces (Fig. 1b). The first-layer a-Si metasurface was fabricated through thermal NIL, lift-off, followed by sequential dry etching with a SiO_2 hard mask, creating mm-scaled nano-structures on fused silica in a single step. Uniquely, a second UV-NIL step was designed to simultaneously achieve multiple functions. First, with a NIL mold it creates a nanograting topography in the UV resist, which serves as the scaffold to produce the vertically coupled aluminum double-layered gratings (VCADGs) by a following metal evaporation. This VCADG design by MFD-NIL eliminates aluminum etching, thus improving the fabrication yield and throughput. Second, the UV NIL resist, with an optical index very close to SiO_2, also acts as the spacer layer between the two metasurfaces, thus eliminating spacer layer deposition. Third, the NIL process also fills the space between the a-Si metasurface structures with low-viscosity UV resist and flattens the surfaces, thus eliminating surface roughness without any additional planarization steps. The unit pixels of fabricated metasurfaces, containing nano-scale a-Si and Al lines at different angles, were inspected by scanning electron microscopy (SEM) (Fig. 2a). Noticeably, the standard deviations of all the measured linewidth of each unit pixel were all smaller than 5 nm, indicating good uniformity. The fabricated samples (4 mm × 5.2 mm nano-patterned area) consist of over 43,000 super-pixels (each containing 8-individual pixels, Fig. 2b). Further, using Morrie fringe patterns as alignment marks, we obtained a high alignment accuracy of <200 nm between the two layers during NIL, thus enabling precise multi-layer stacking.

The fabricated device was diced, and bonded onto a CMOS sensor for optical characterization (Fig. 3b). Noticeably, the measured LP extinction ratio (LPER), averaging 60 from 530 nm to 620 nm (Fig. 3c), was ~3 times better compared to EBL fabricated device [1]. Similarly, the CPER was found 80, or 4 times better than EBL-made device. We expect that this demonstration will open a new venue for fabrication and integration of metasurfaces in various applications such as metalens, augmented reality, and holographic applications.

[1] J. Zuo et al., "Chip-integrated full-stokes polarimetric CMOS imaging sensor", In CLEO: Science and Innovations (pp. SF2K-5) (2022).

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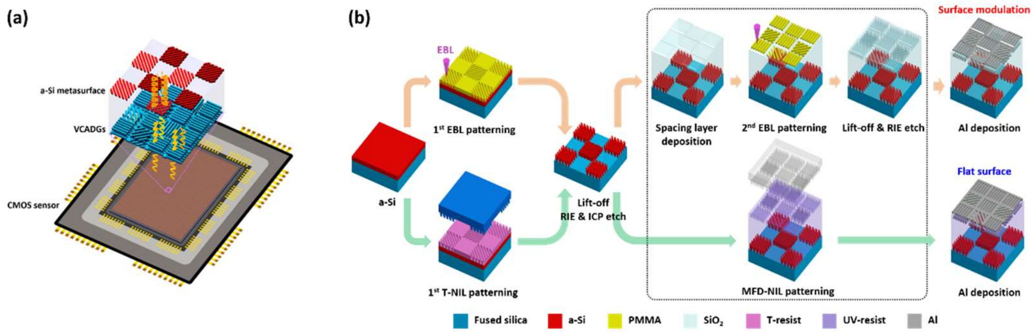

Fig 1. Chip-integrated polarimetric CMOS imaging sensor using NIL process. (a) Conceptual 3D schematic illustration of the desired structures. (b) Schematic illustration of two different fabrication processes for double-layer chiral metasurfaces (DLCMs). (Orange arrow) Conventional fabrication process based on EBL. (Green arrow) Developed multi-functional-direct (MFD)-NIL process.

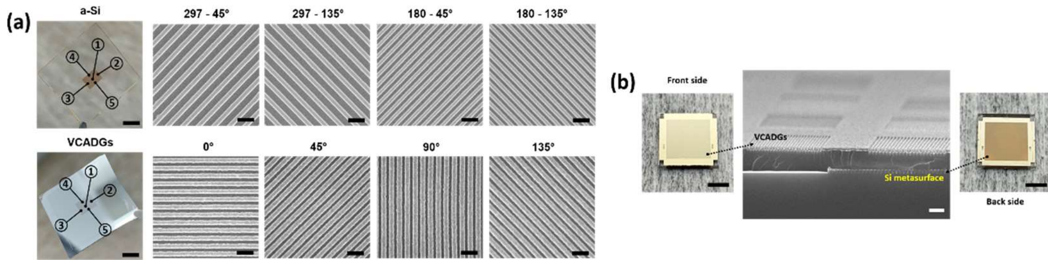

Fig 2. Individual and integrated metasurfaces. (a) Photographic (scale bar: 5 mm) and SEM images (scale bar: 300 nm) of fabricated a-Si metasurface (top) and VCADGs (bottom) for uniformity study. (b) Cross-sectional SEM image (middle, scale bar: 1 μm) and photographic images (left: front & right: back, scale bar: 3 mm) of the integrated DLCMs.

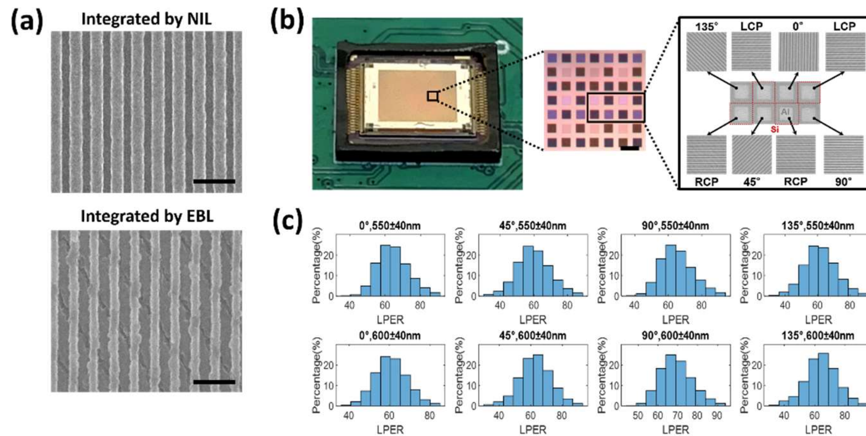

Fig. 3. Optical performance of the device. (a) SEM images of the integrated DLCMs by the NIL process (top) and the EBL-based process (bottom) [2]. Scale bar: 300 nm. (b) The photographic image of the device bonded onto CMOS (left), microscopic image of integrated DLCMs (middle, scale bar: 10 μm), and magnified SEM images of individual super-pixel (right). (c) Wavelength and angle dependent LPER distribution.